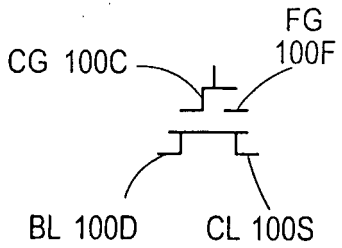
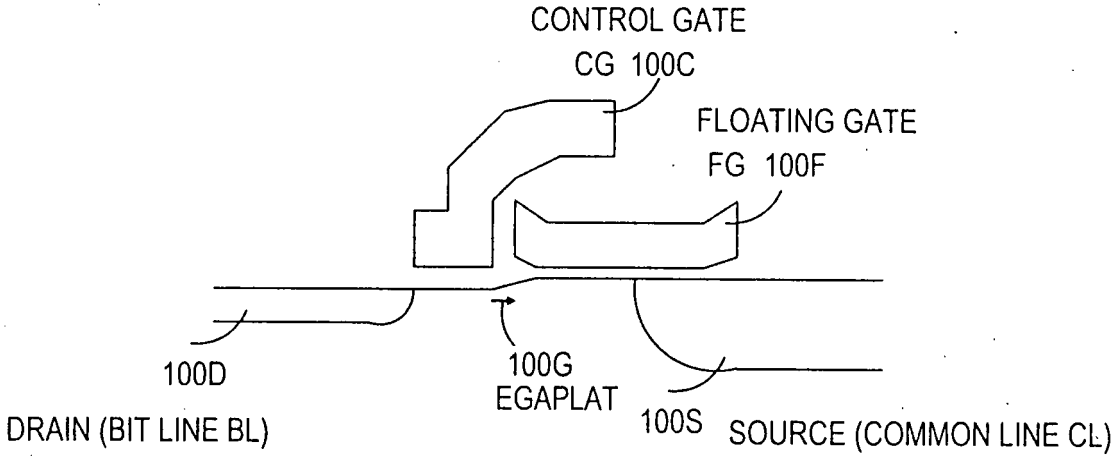
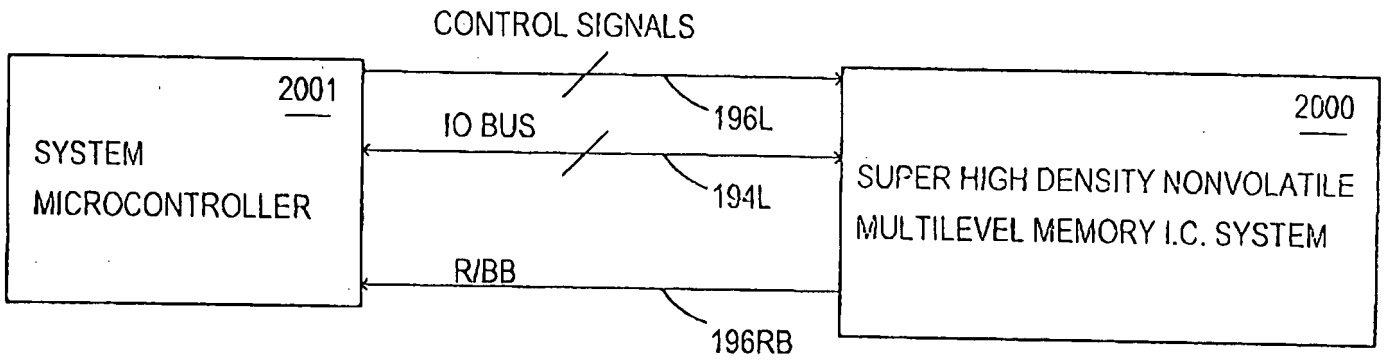


FIGURE 1B



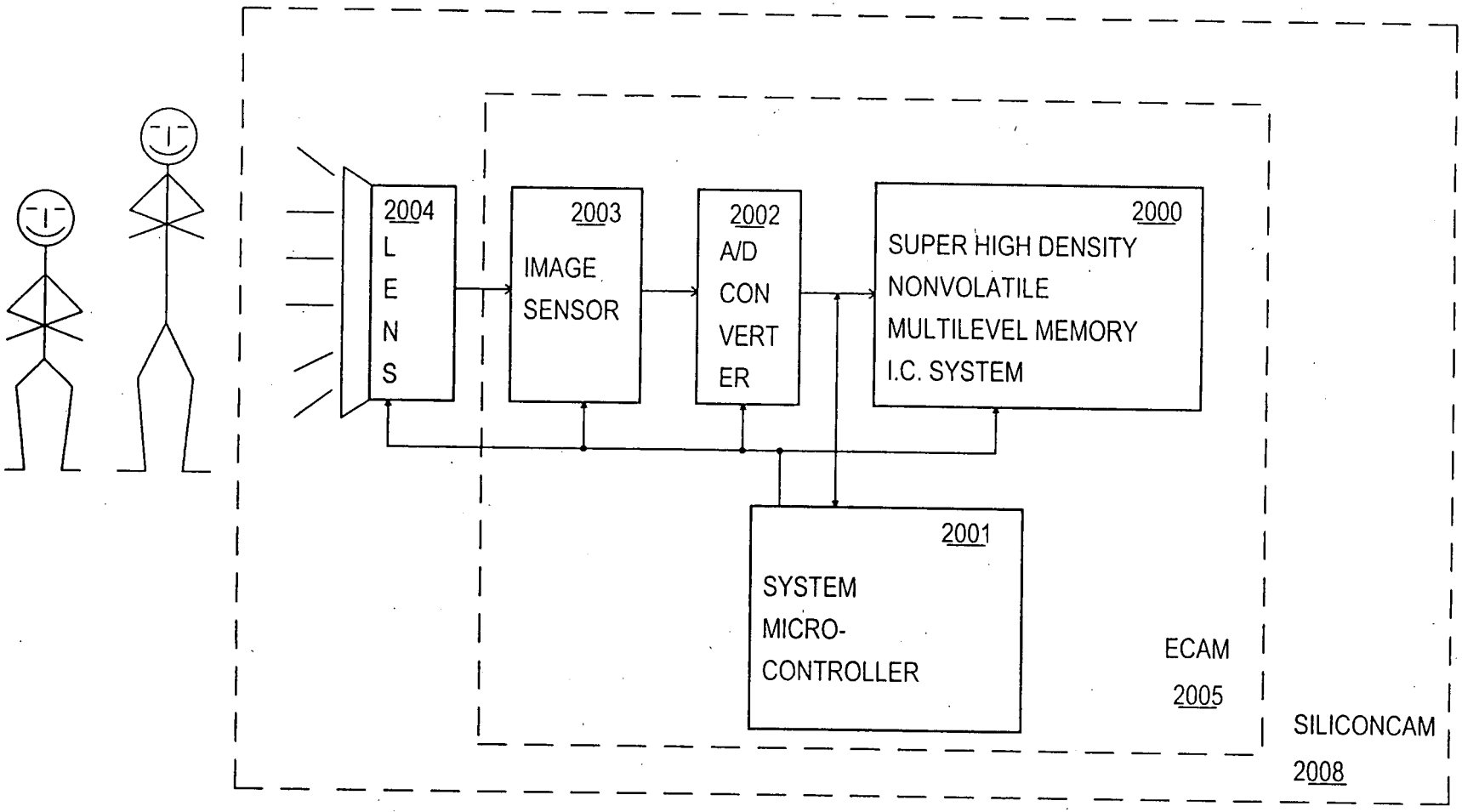
SOURCE SIDE INJECTION FLASH MEMORY CELL: CROSS SECTION ALONG THE BIT LINE

FIGURE 1A



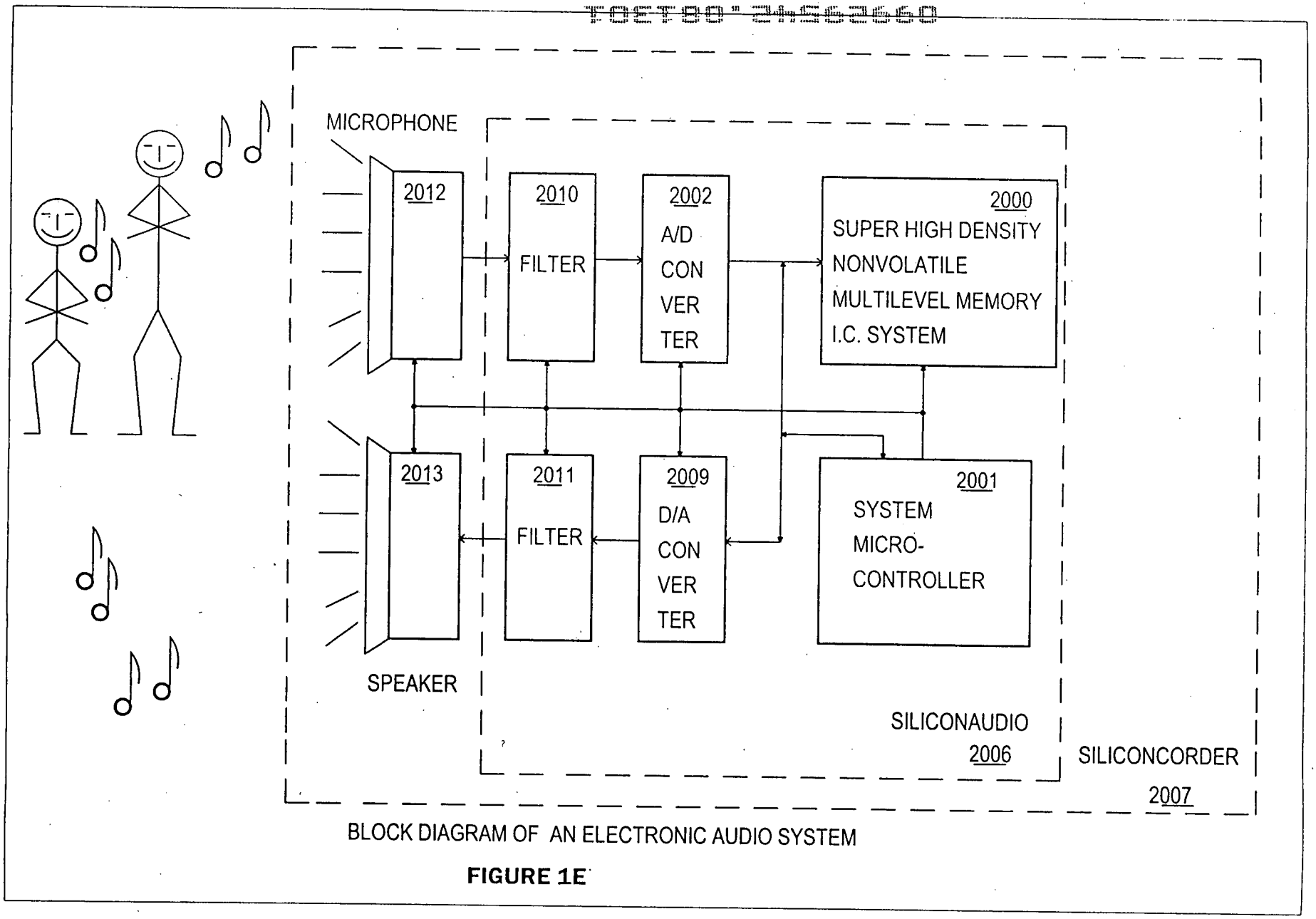
BLOCK DIAGRAM OF A NONVOLATILE MULTILEVEL MEMORY SYSTEM

FIGURE 1C



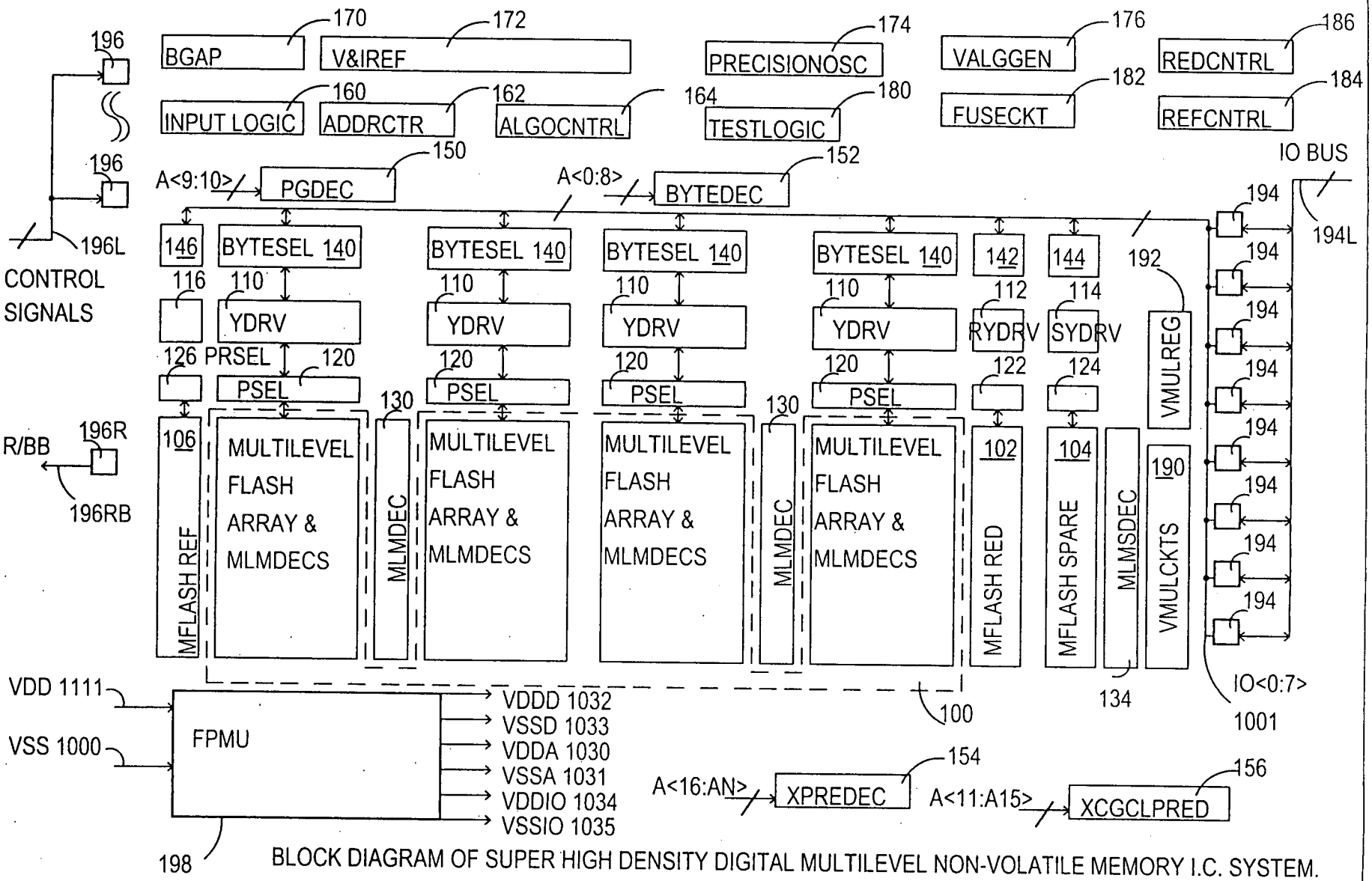
BLOCK DIAGRAM OF AN ELECTRONIC CAMERA SYSTEM

FIGURE 1D



BLOCK DIAGRAM OF AN ELECTRONIC AUDIO SYSTEM

FIGURE 1E



BLOCK DIAGRAM OF SUPER HIGH DENSITY DIGITAL MULTILEVEL NON-VOLATILE MEMORY I.C. SYSTEM.

FIGURE 2A

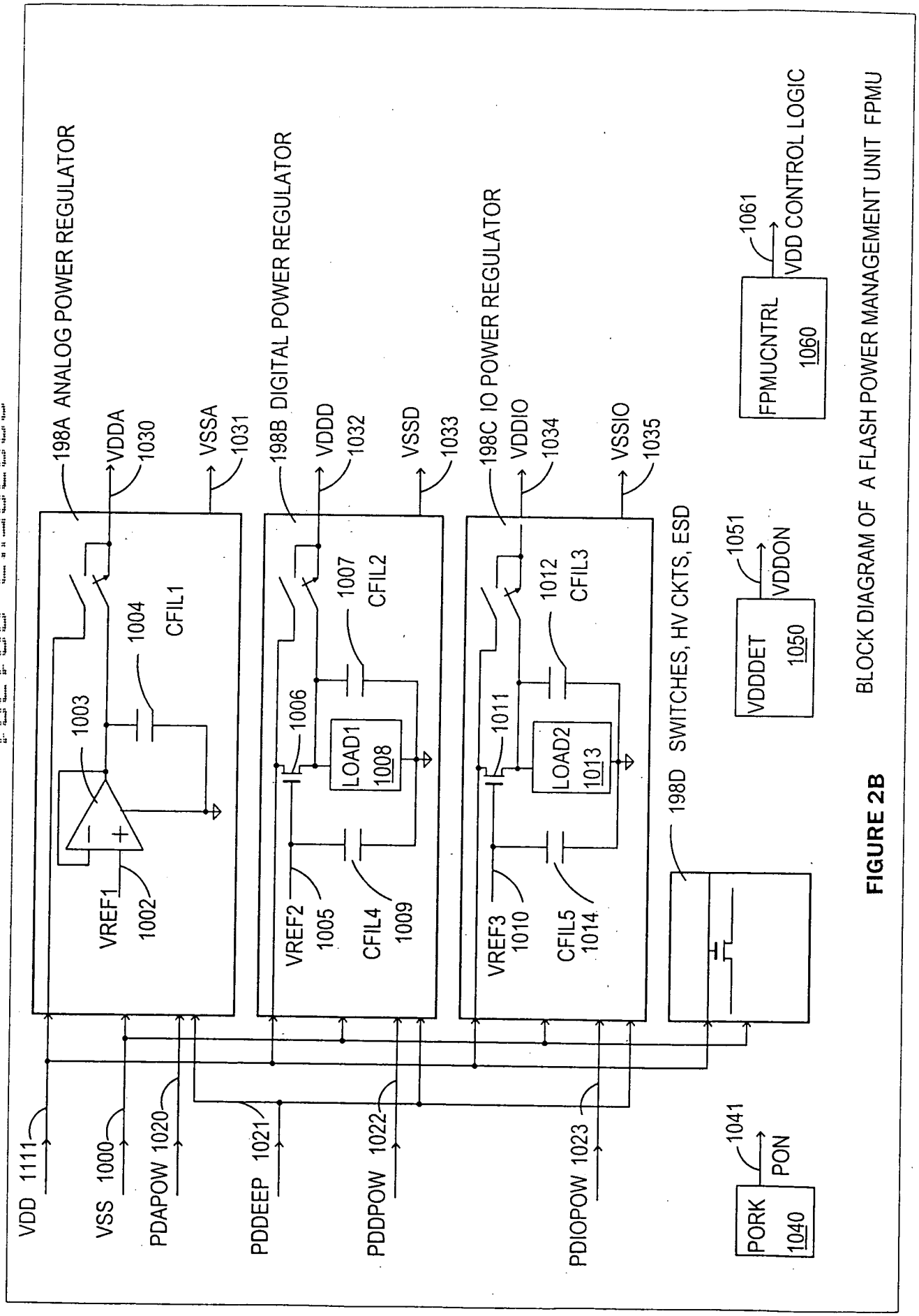
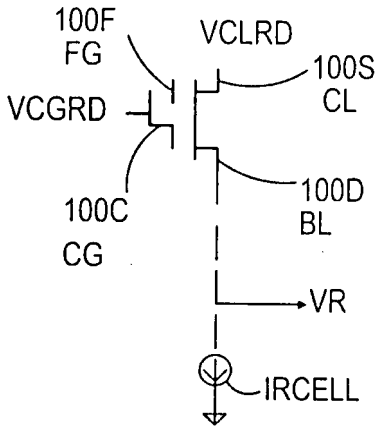
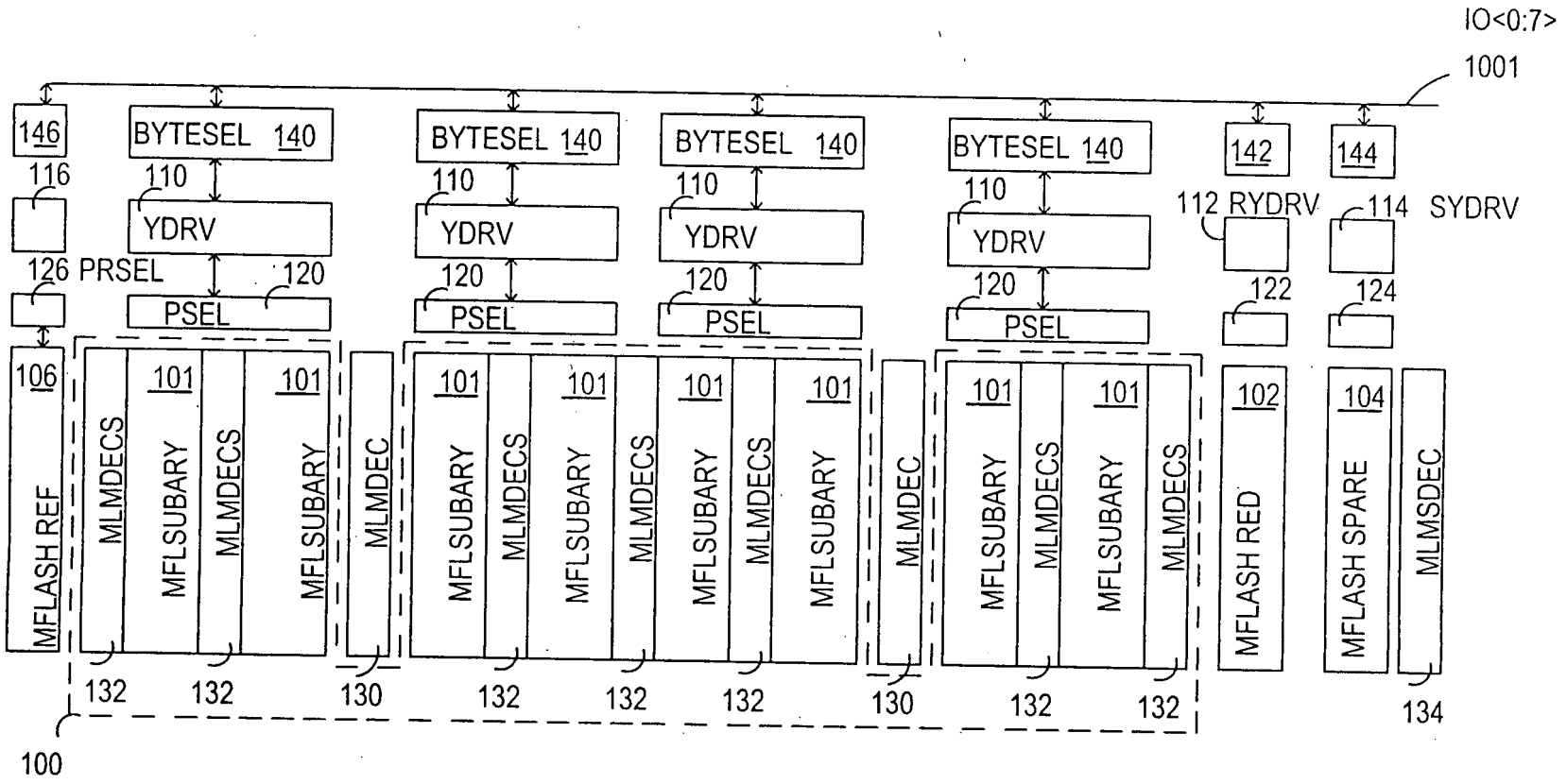


FIGURE 2B BLOCK DIAGRAM OF A FLASH POWER MANAGEMENT UNIT FPMU



VOLTAGE MODE SENSING

FIGURE 2C



BLOCK DIAGRAM OF SUPER HIGH DENSITY DIGITAL MULTILEVEL NON-VOLATILE MEMORY ARRAY ARCHITECTURE

FIGURE 3A

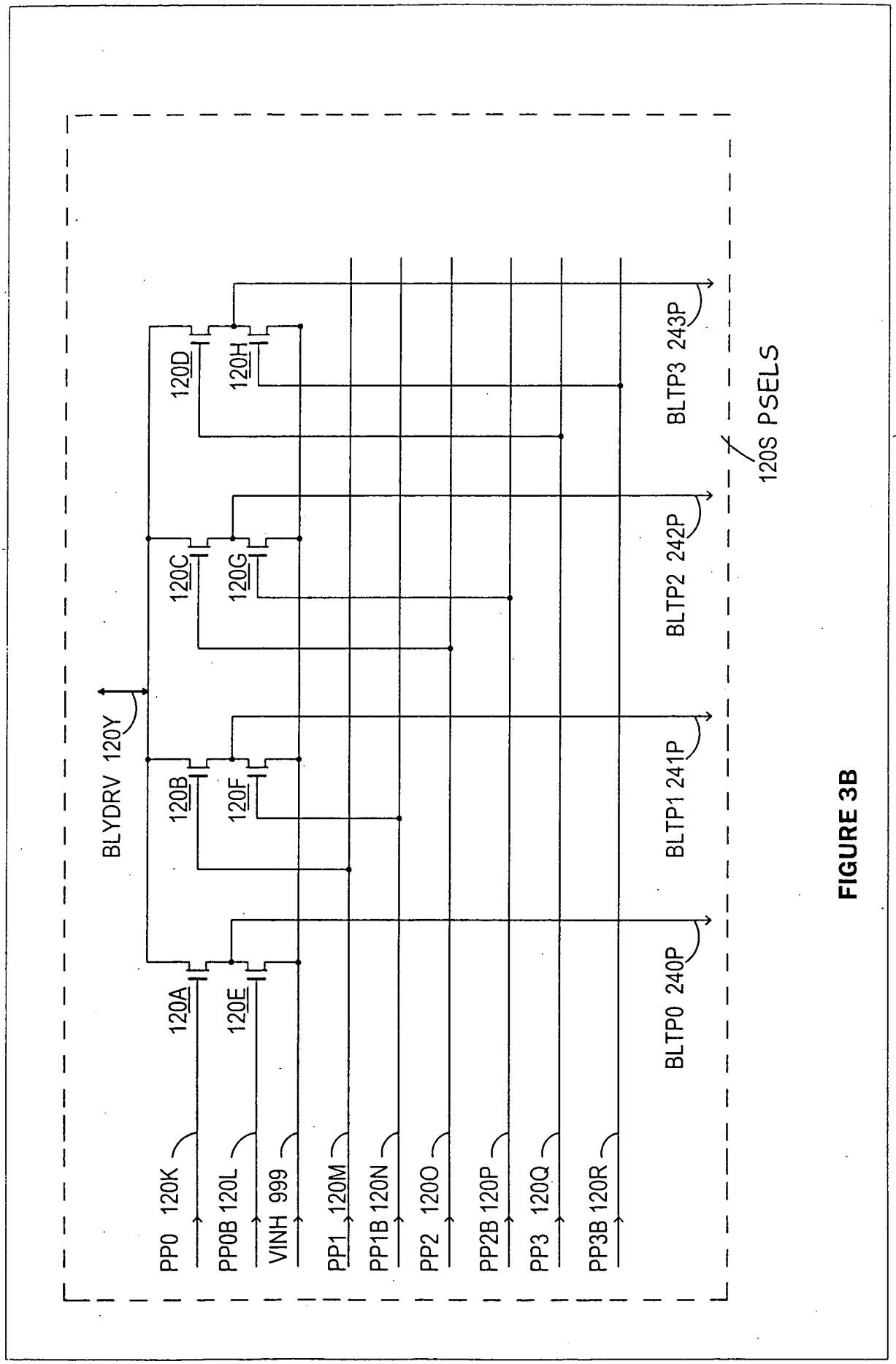

PP0 120K
PP0B 120L
VINH 999
PP1 120M
PP1B 120N
PP2 120O
PP2B 120P
PP3 120Q
PP3B 120R
BLYDRV 120Y
120A
120B
120C
120D
120E
120F
120G
120H
BLTP0 240P
BLTP1 241P
BLTP2 242P
BLTP3 243P
120S PSELS

FIGURE 3B

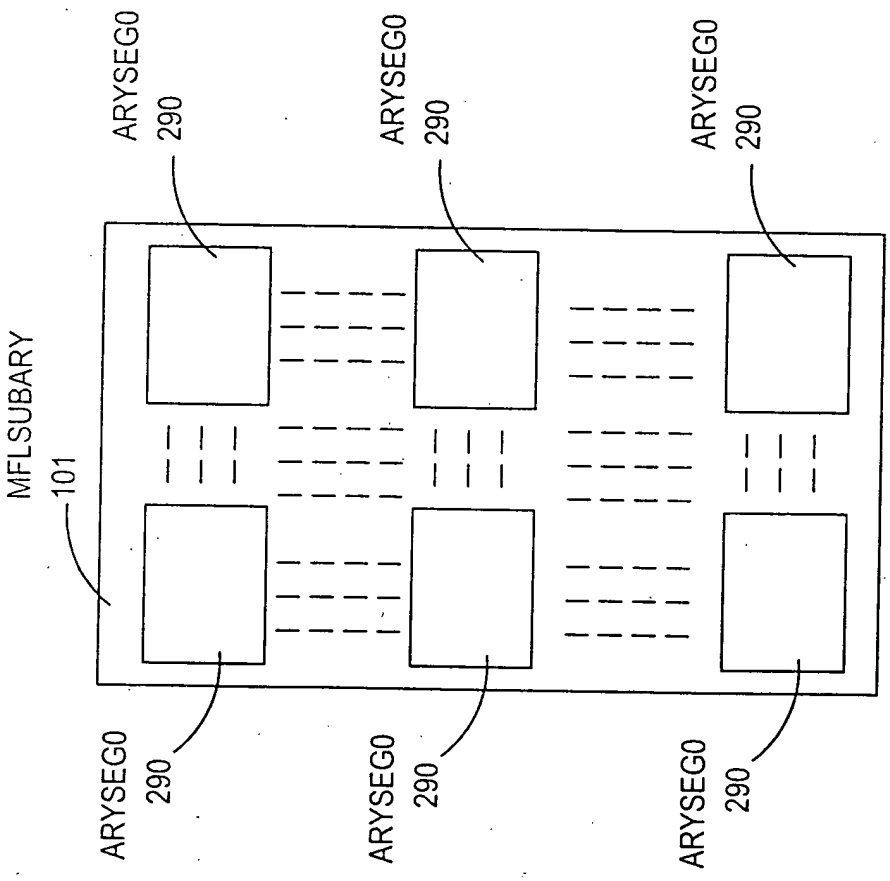

MFLSUBARY
101
ARYSEG0
290
ARYSEG0
290
ARYSEG0
290
ARYSEG0
290
ARYSEG0
290
ARYSEG0
290

FIGURE 3C

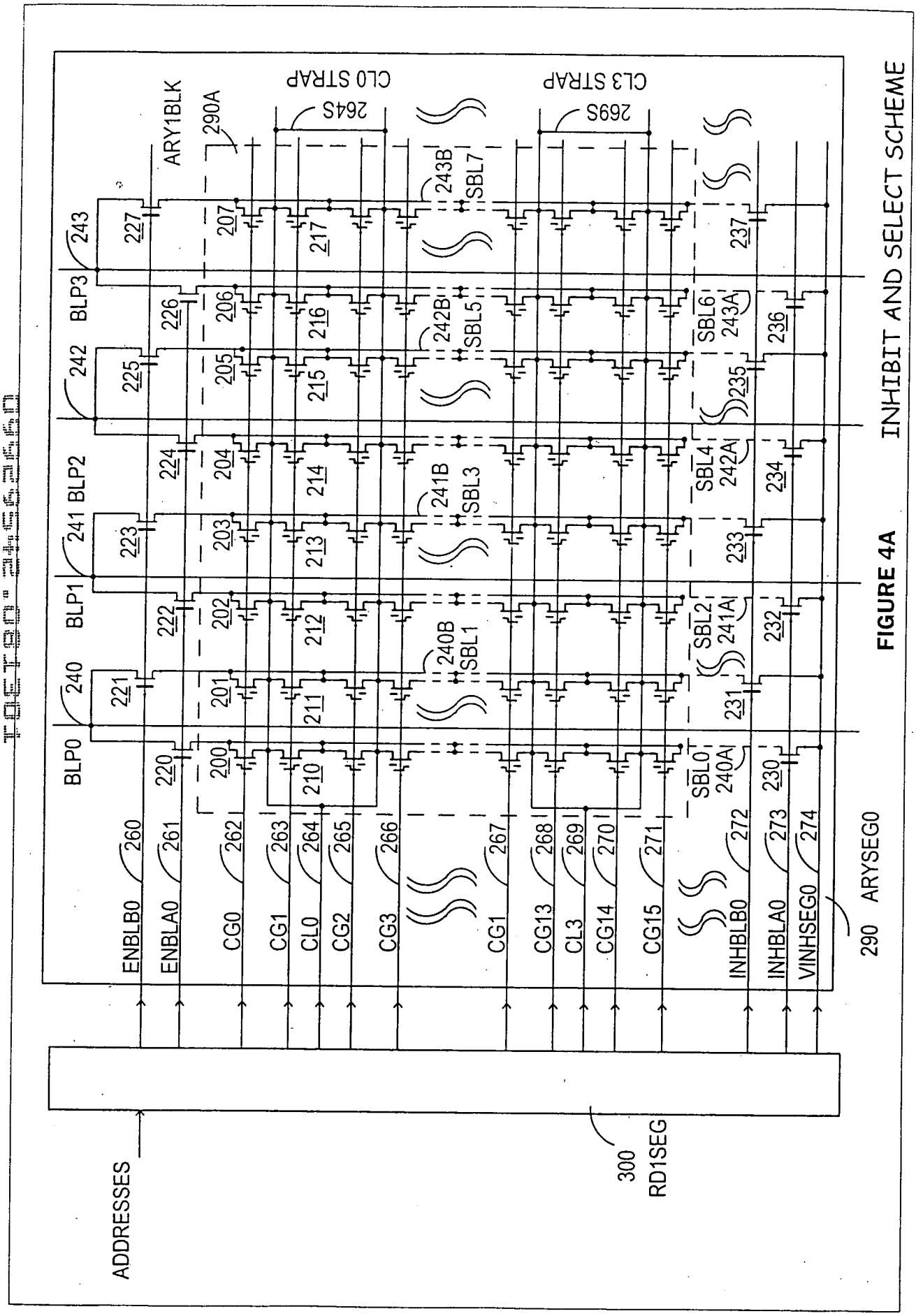


FIGURE 4A INHIBIT AND SELECT SCHEME

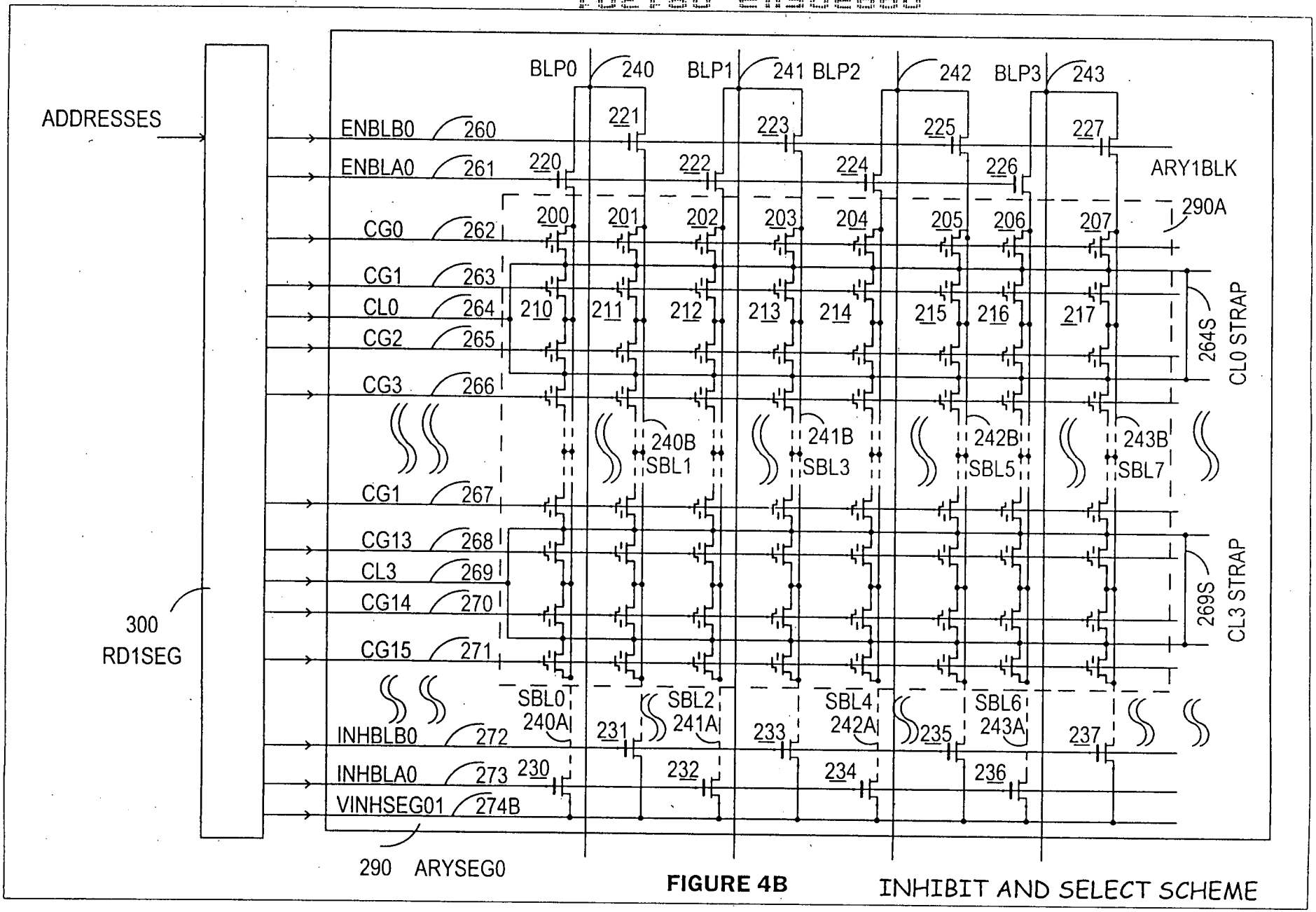


FIGURE 4B INHIBIT AND SELECT SCHEME

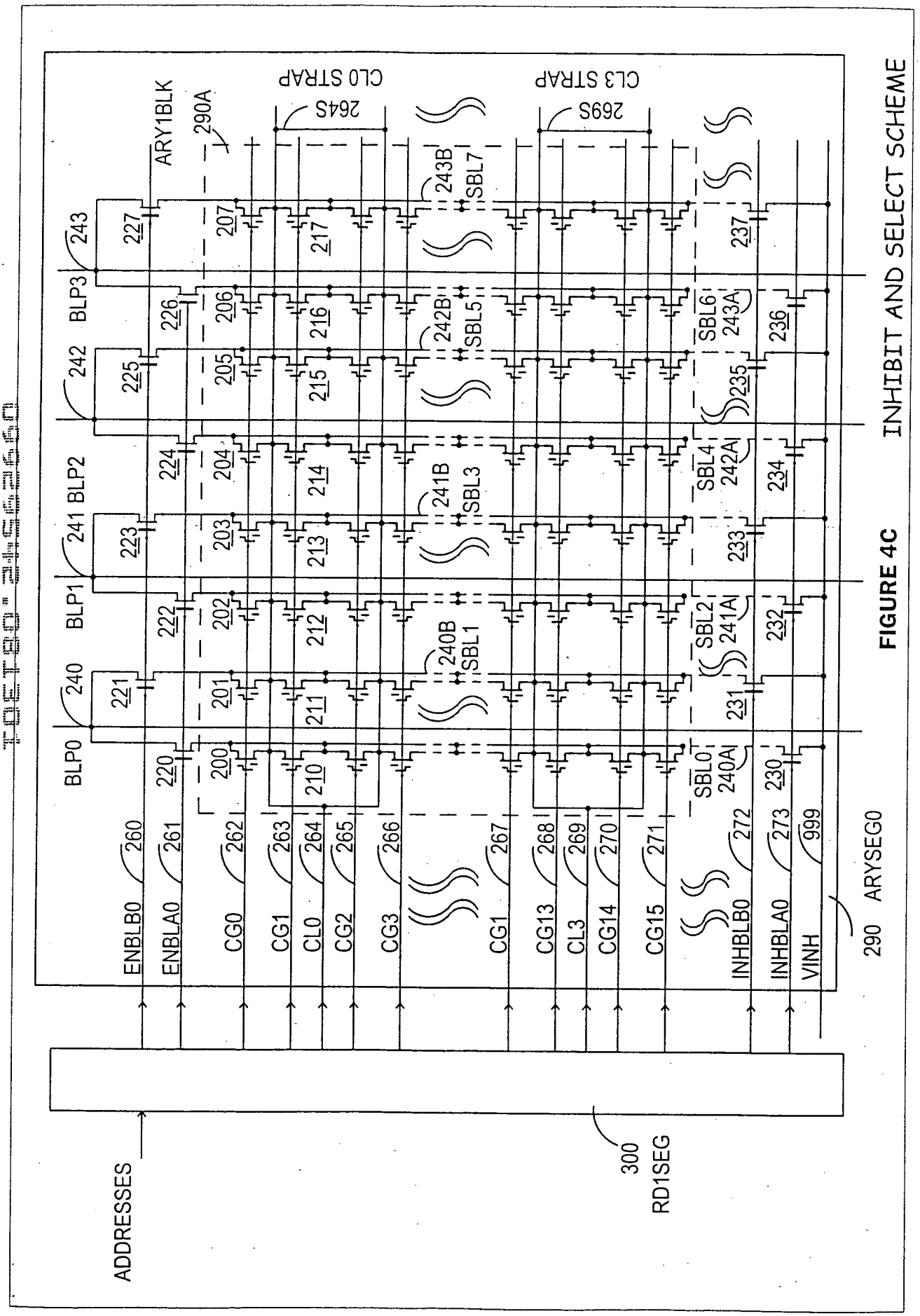


FIGURE 4C INHIBIT AND SELECT SCHEME

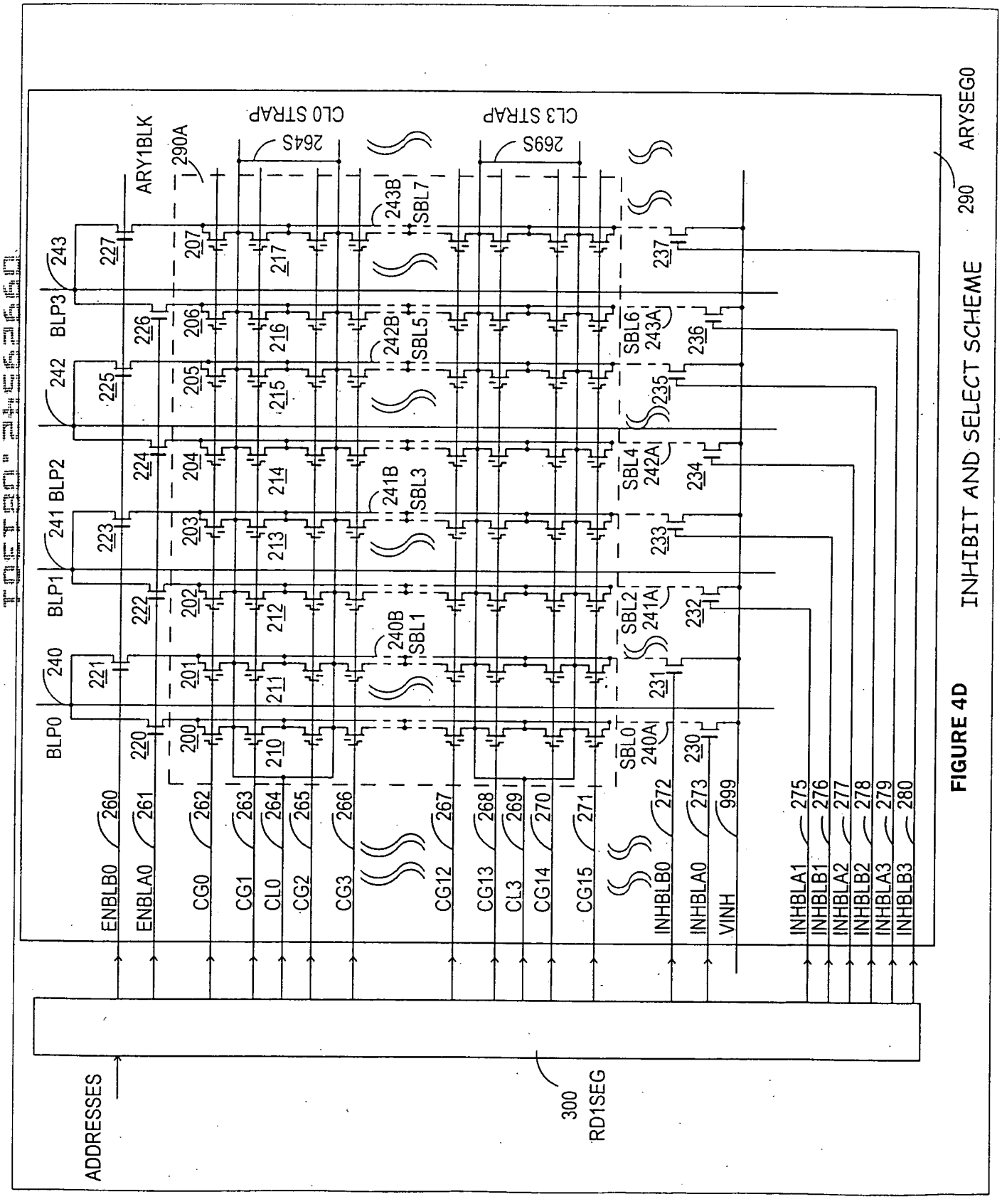


FIGURE 4D INHIBIT AND SELECT SCHEME

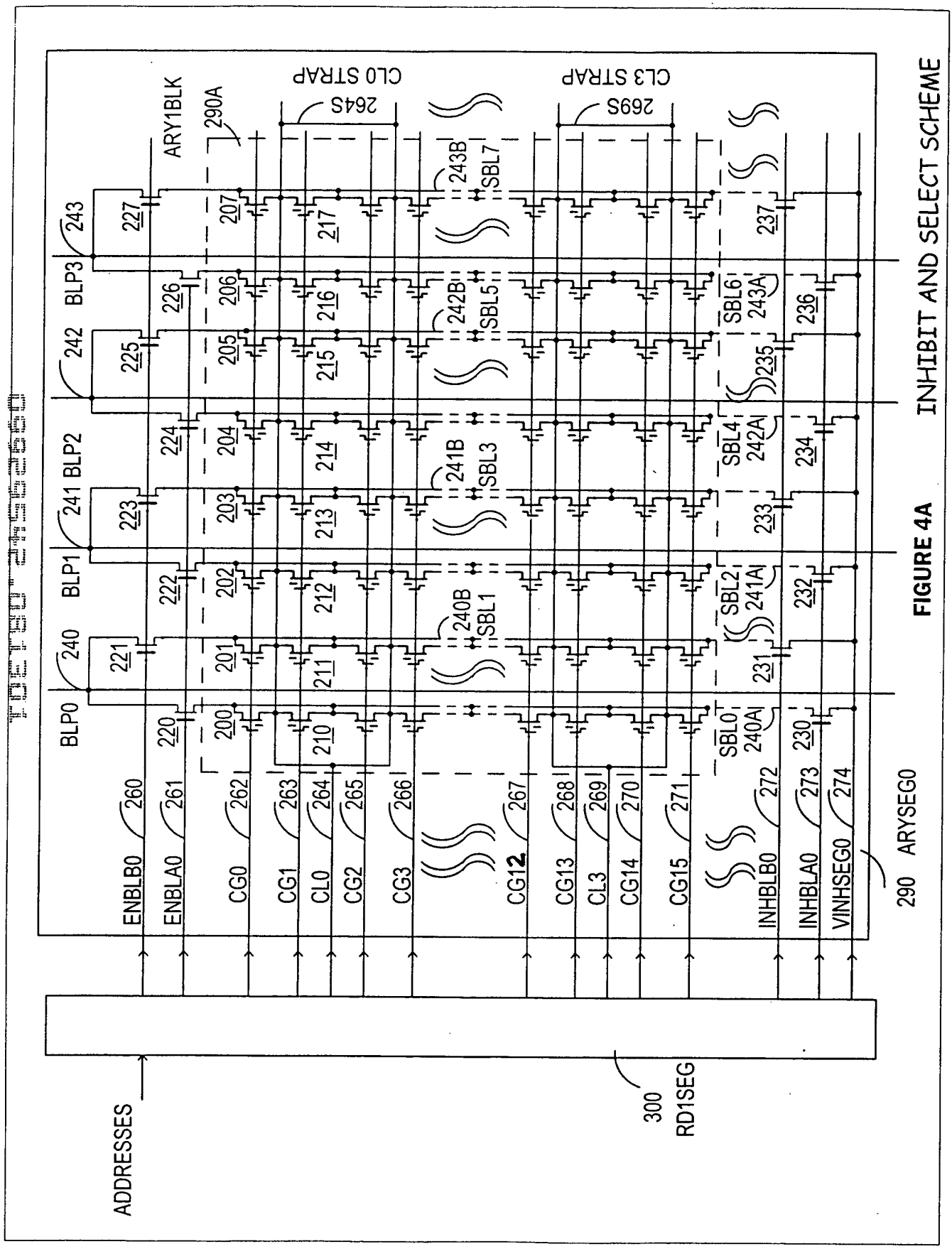


FIGURE 4A INHIBIT AND SELECT SCHEME

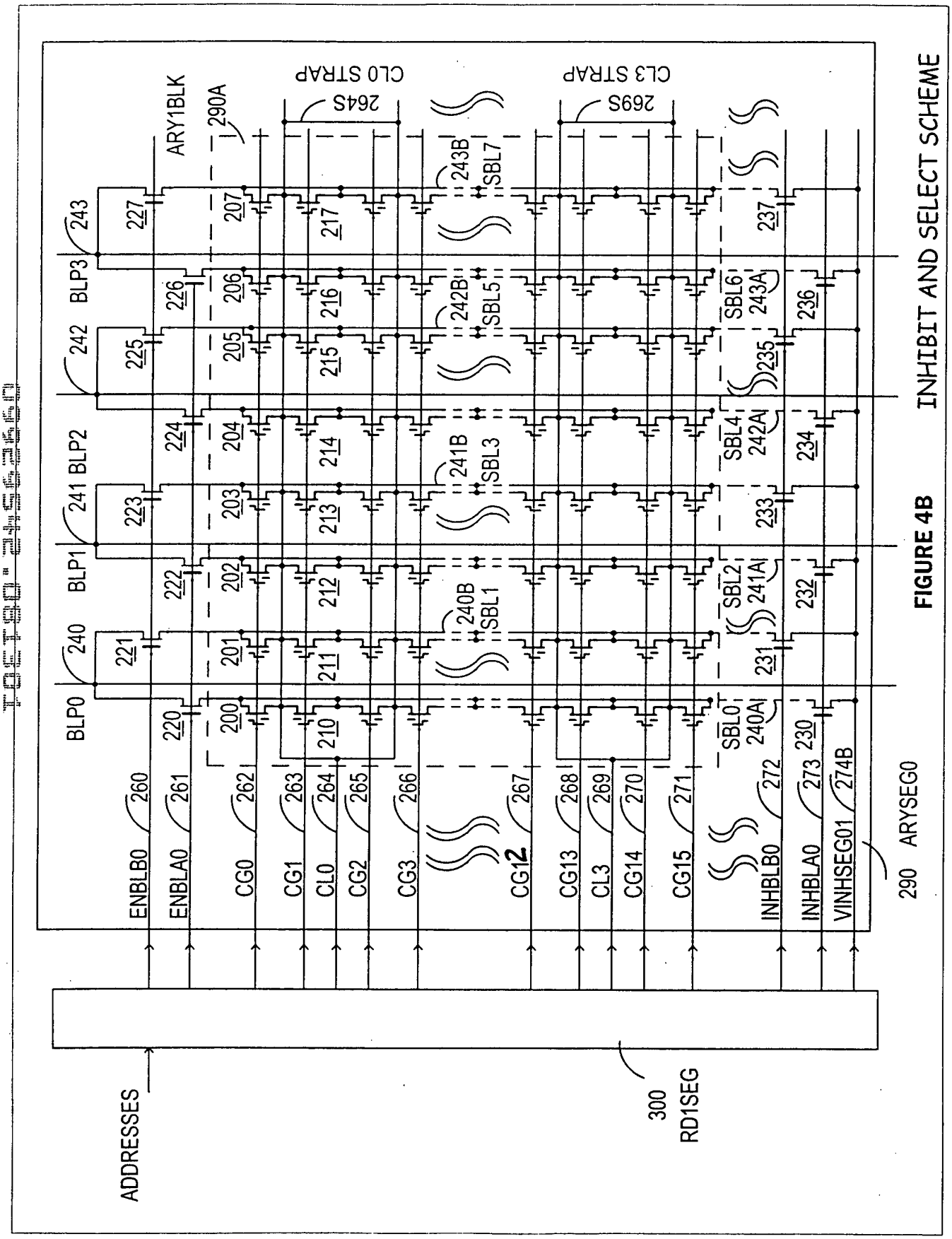


FIGURE 4B INHIBIT AND SELECT SCHEME

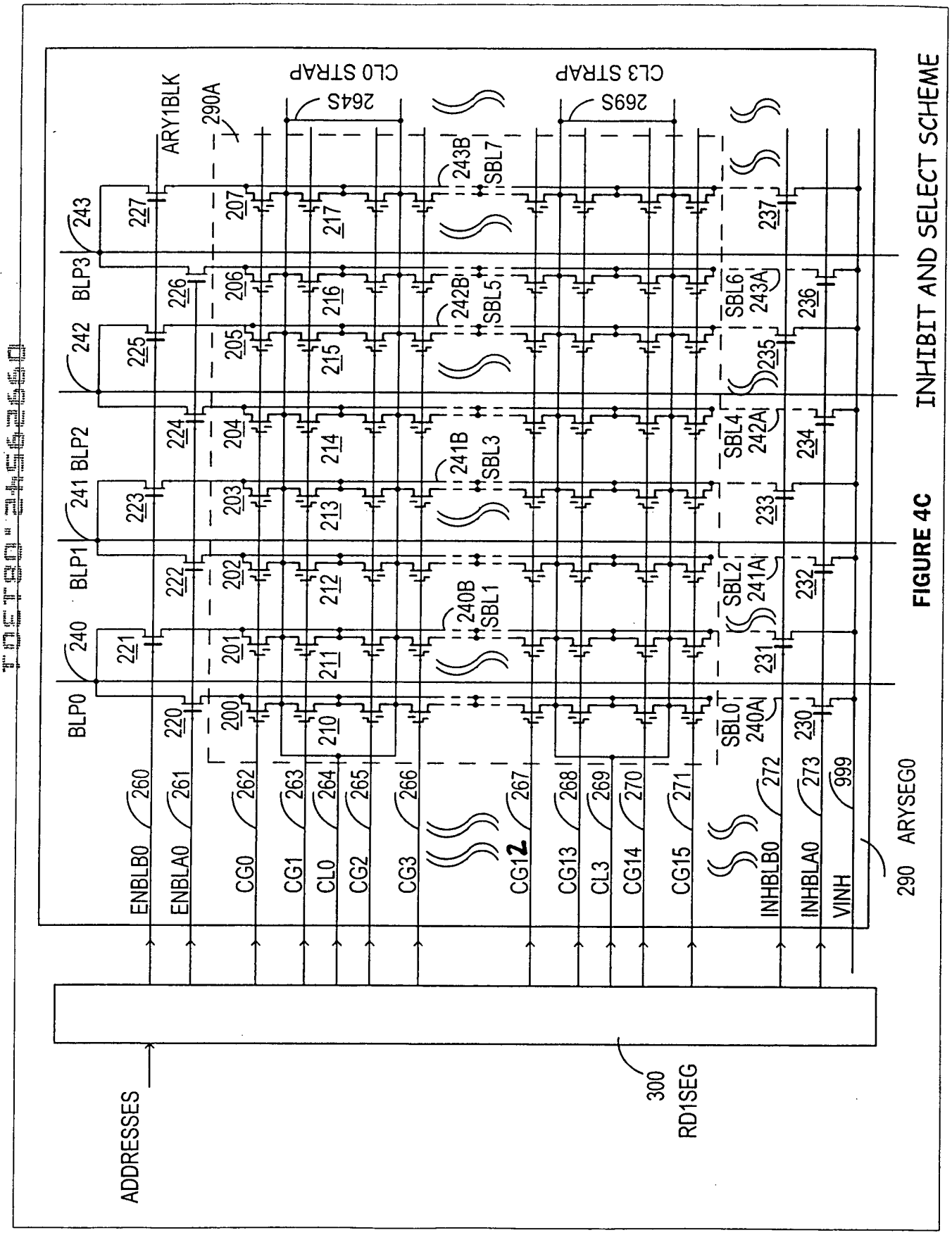


FIGURE 4C INHIBIT AND SELECT SCHEME

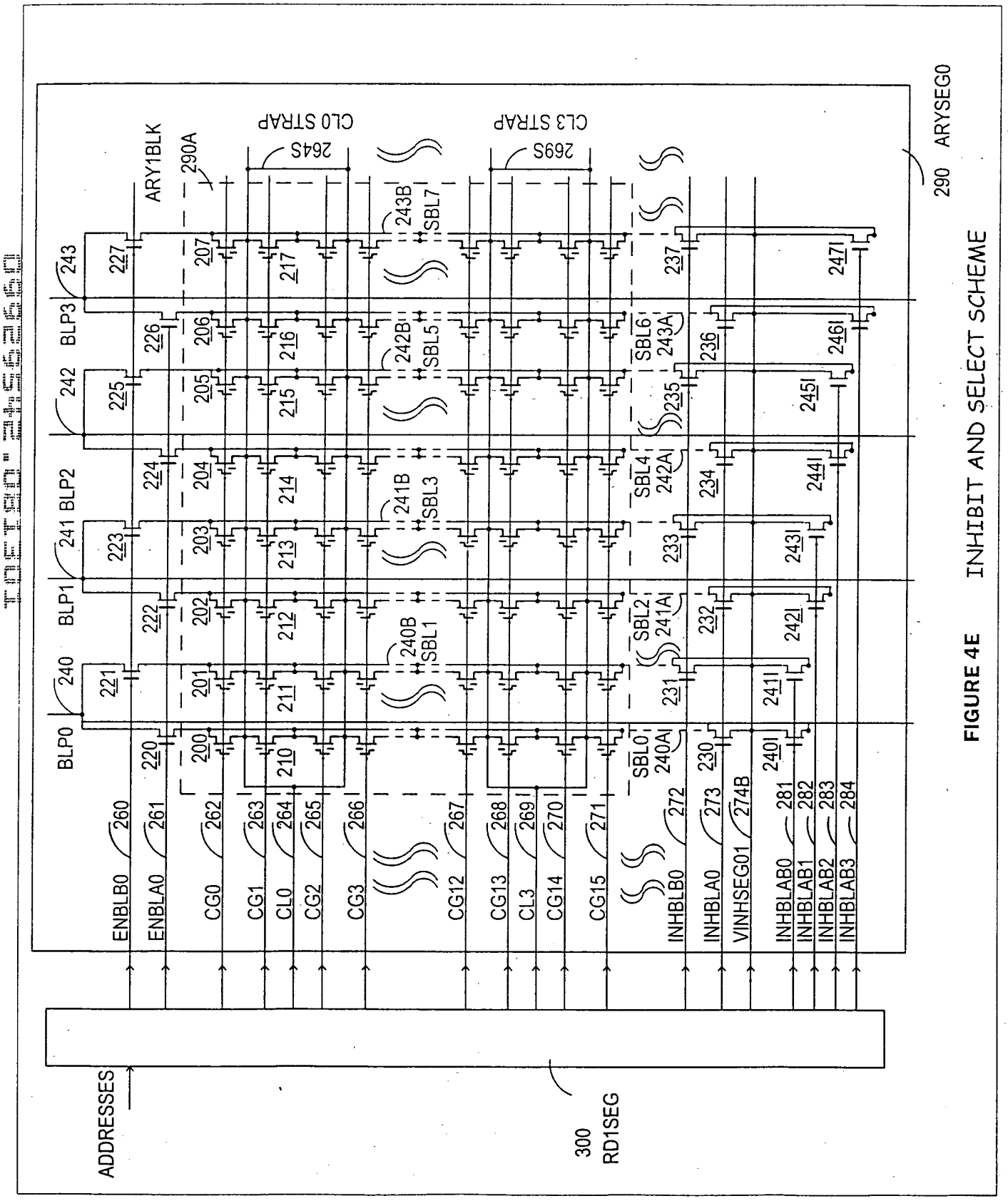


FIGURE 4E INHIBIT AND SELECT SCHEME

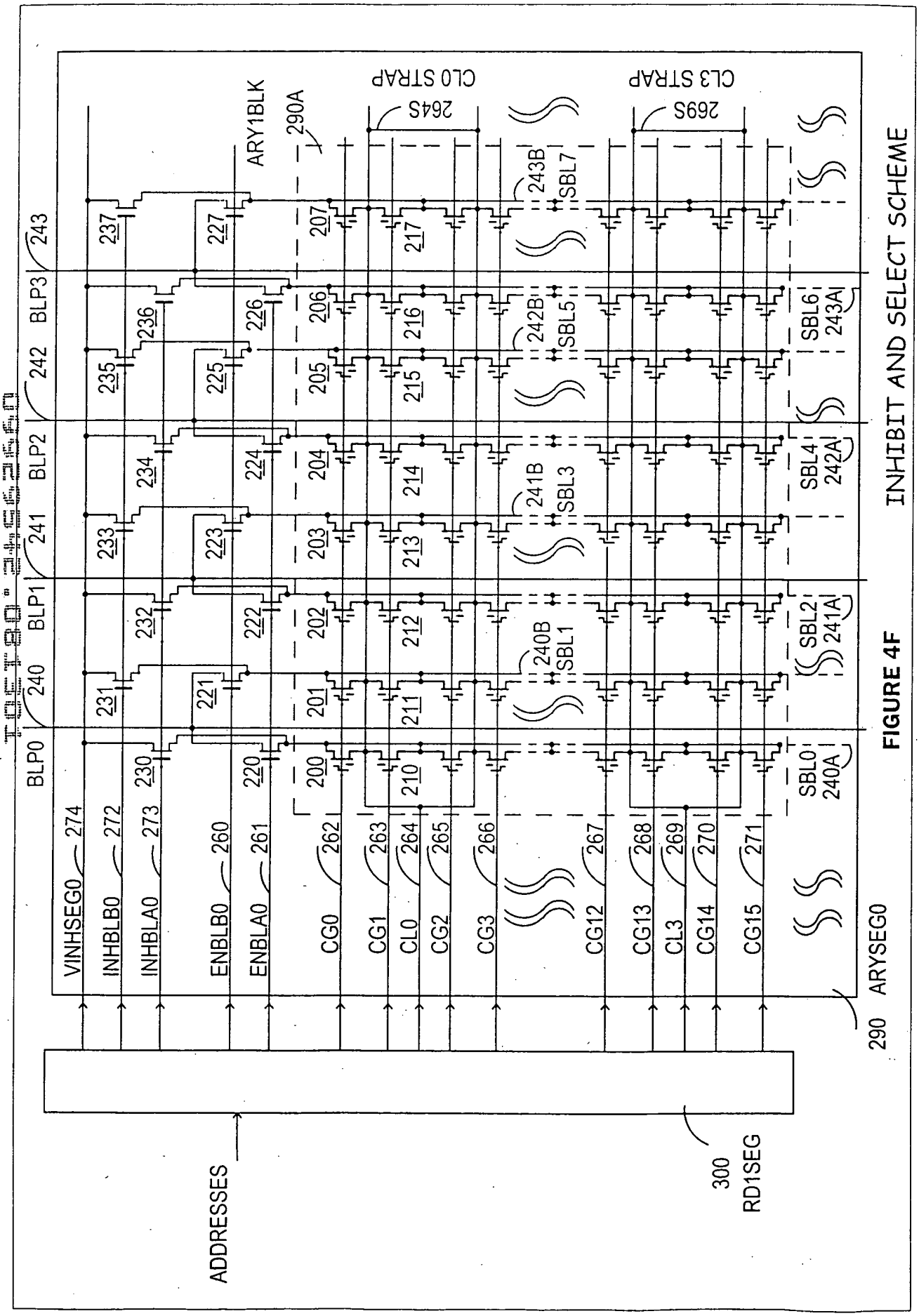
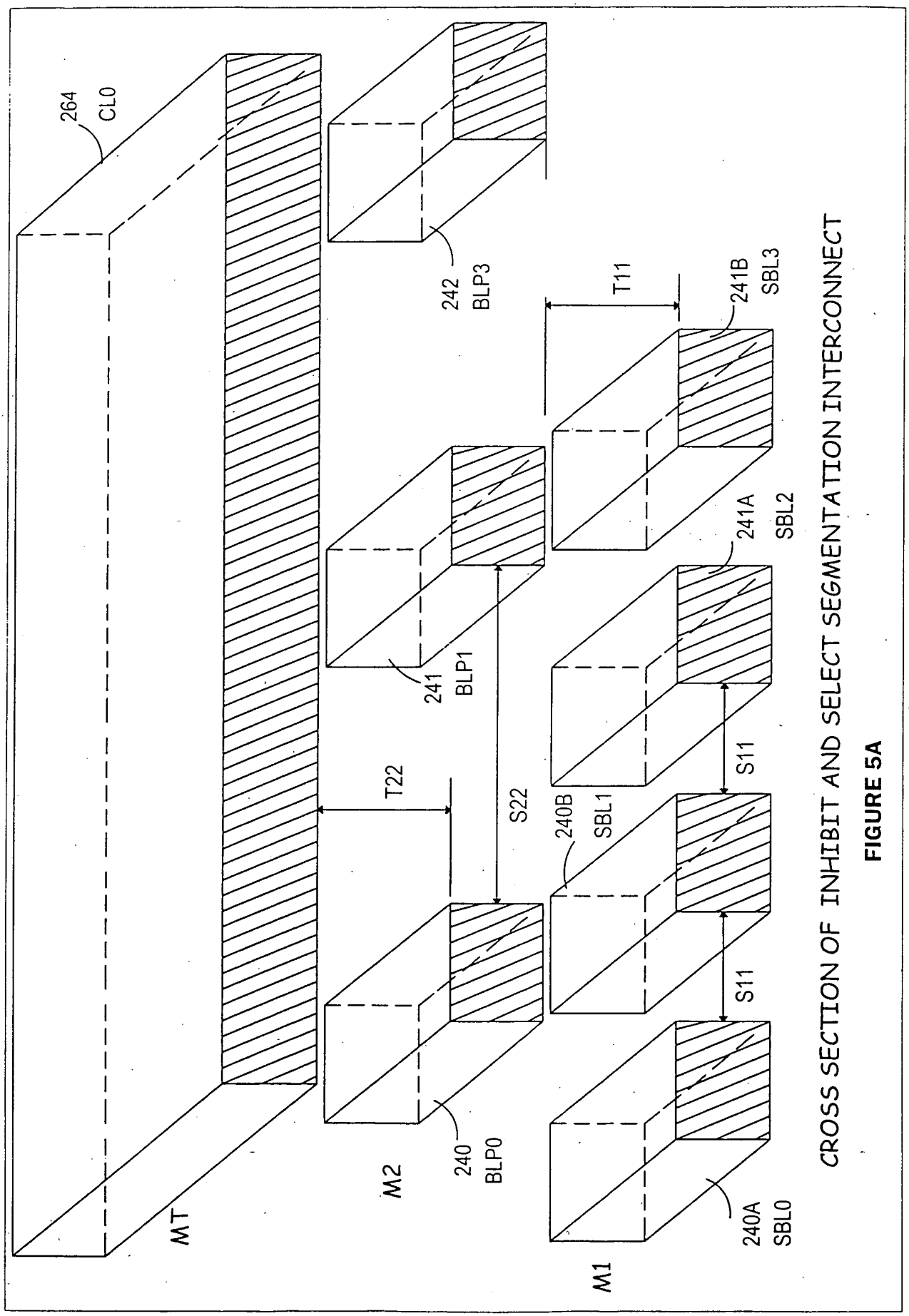
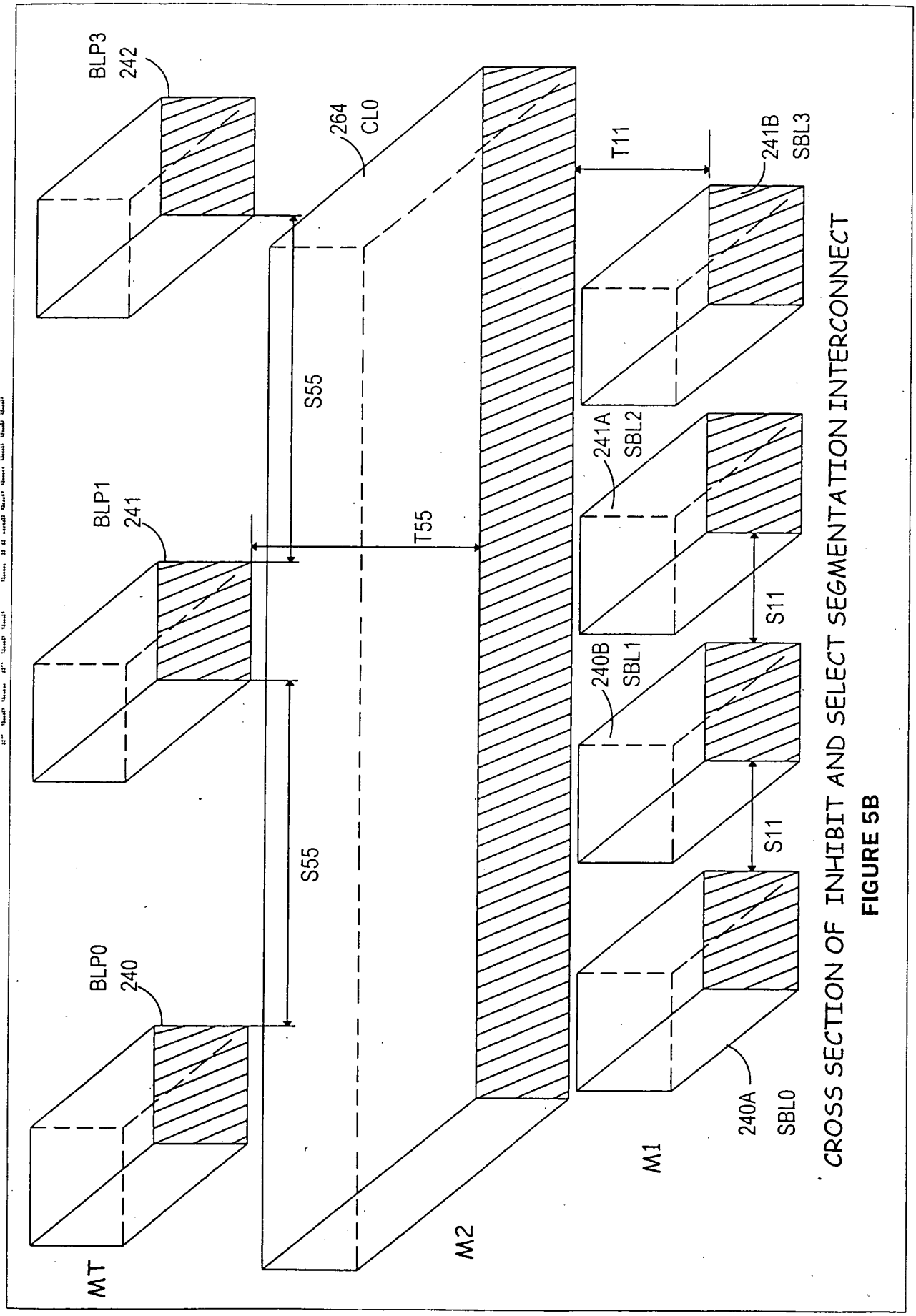


FIGURE 4F INHIBIT AND SELECT SCHEME



CROSS SECTION OF INHIBIT AND SELECT SEGMENTATION INTERCONNECT

FIGURE 5A



CROSS SECTION OF INHIBIT AND SELECT SEGMENTATION INTERCONNECT

FIGURE 5B

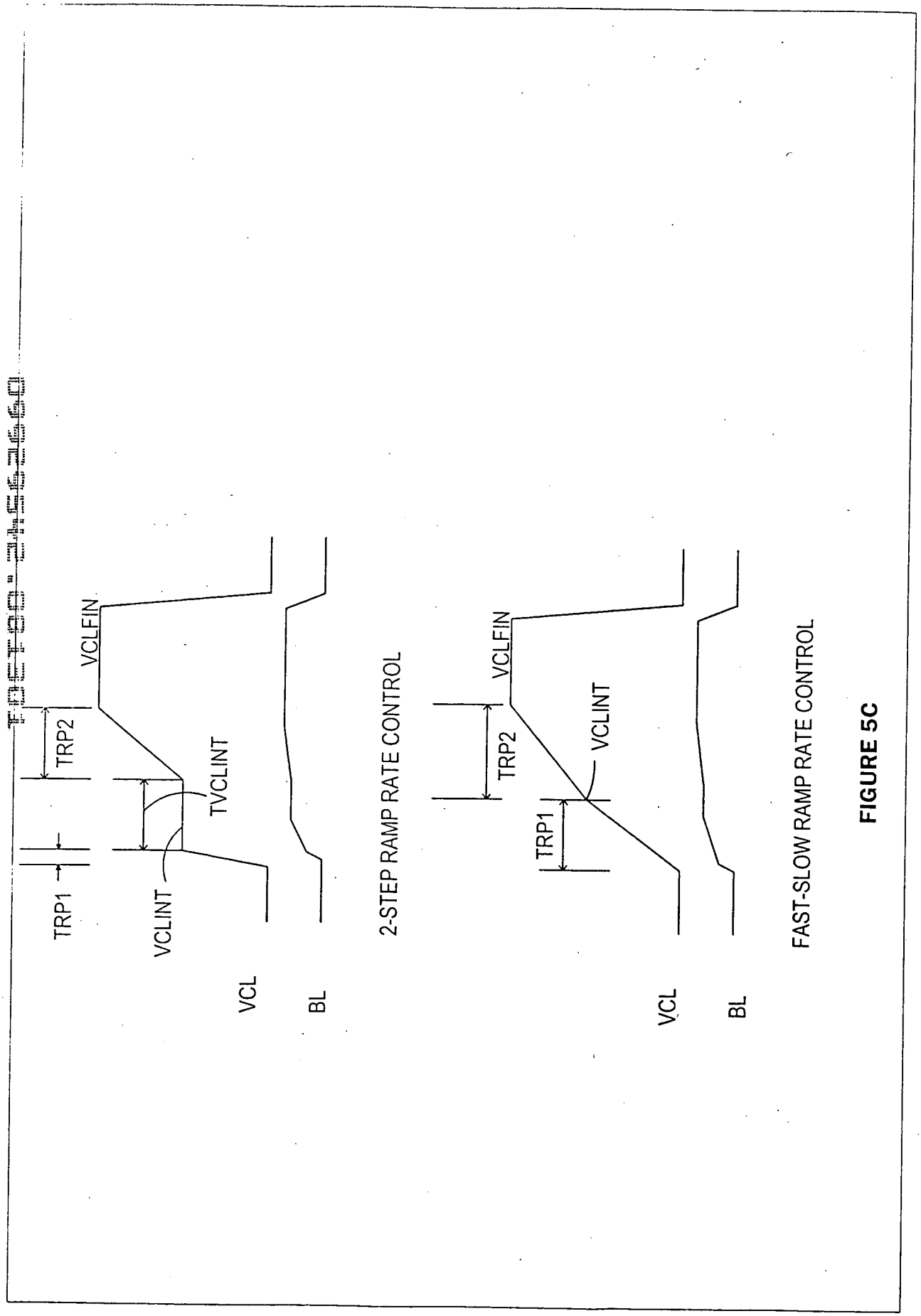

TRP1
TRP2
VCLFIN
TVCLINT
VCLINT
VCL
BL
2-STEP RAMP RATE CONTROL
TRP2
VCLFIN
VCLINT
TRP1
VCL
BL
FAST-SLOW RAMP RATE CONTROL

FIGURE 5C

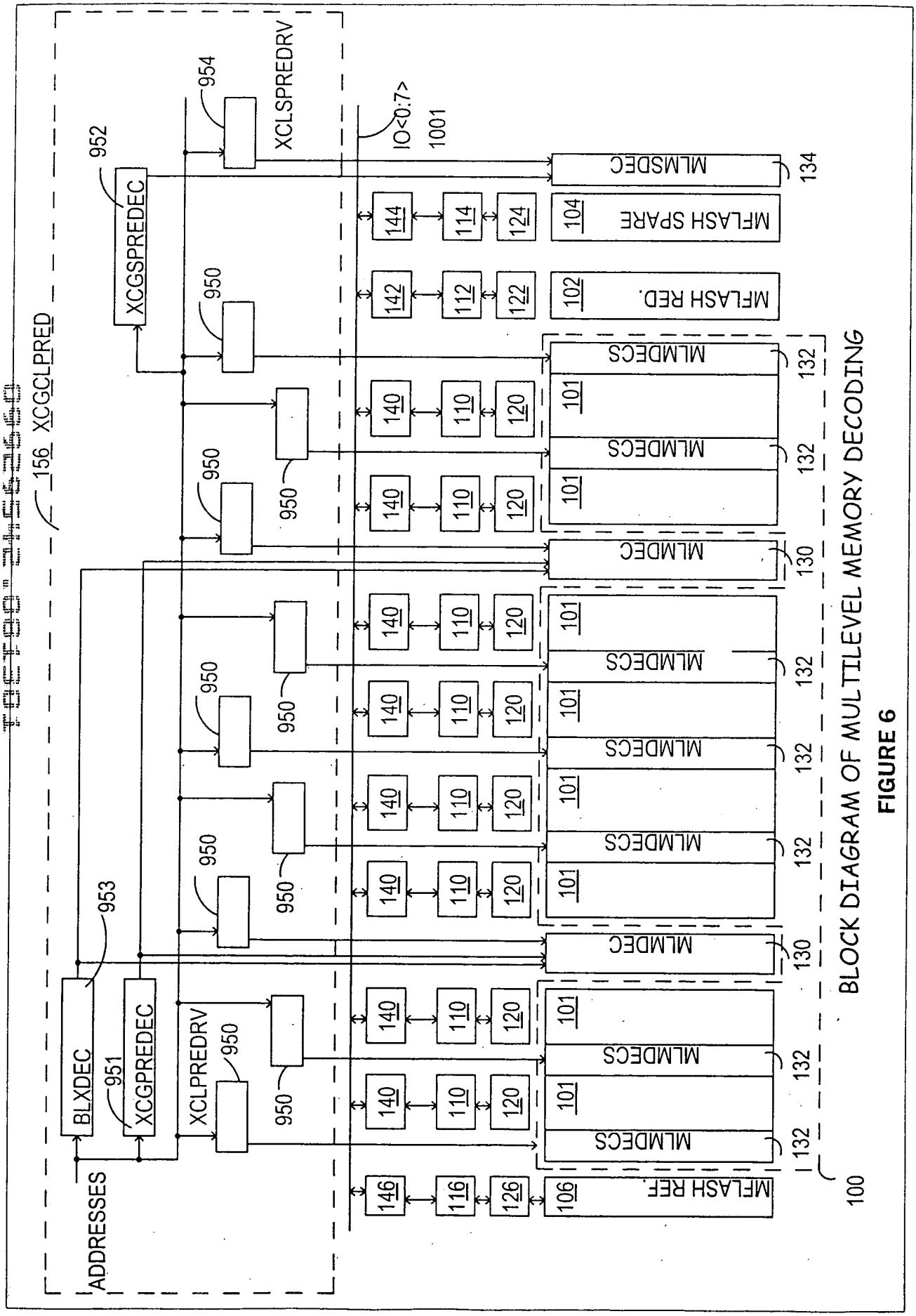
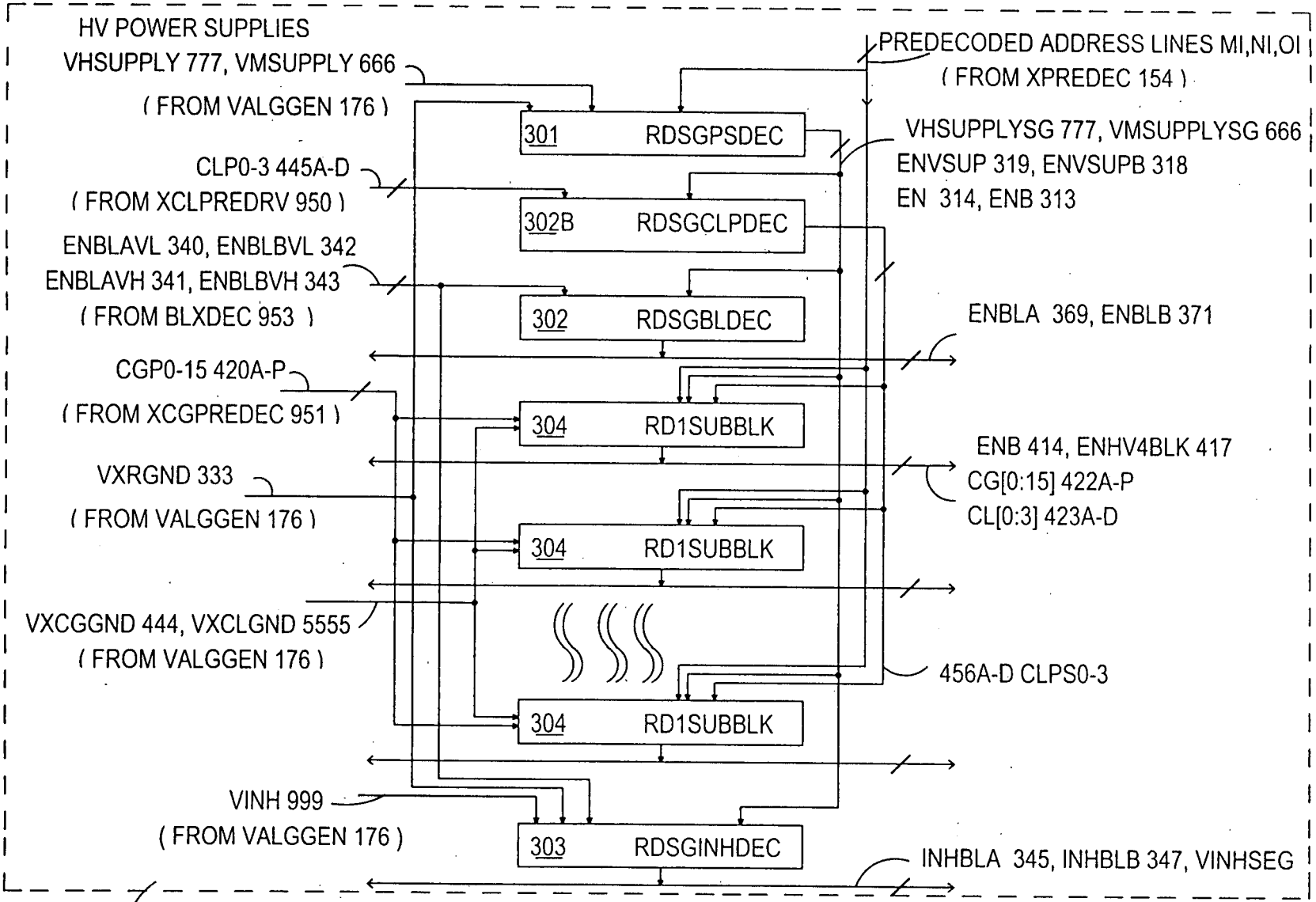
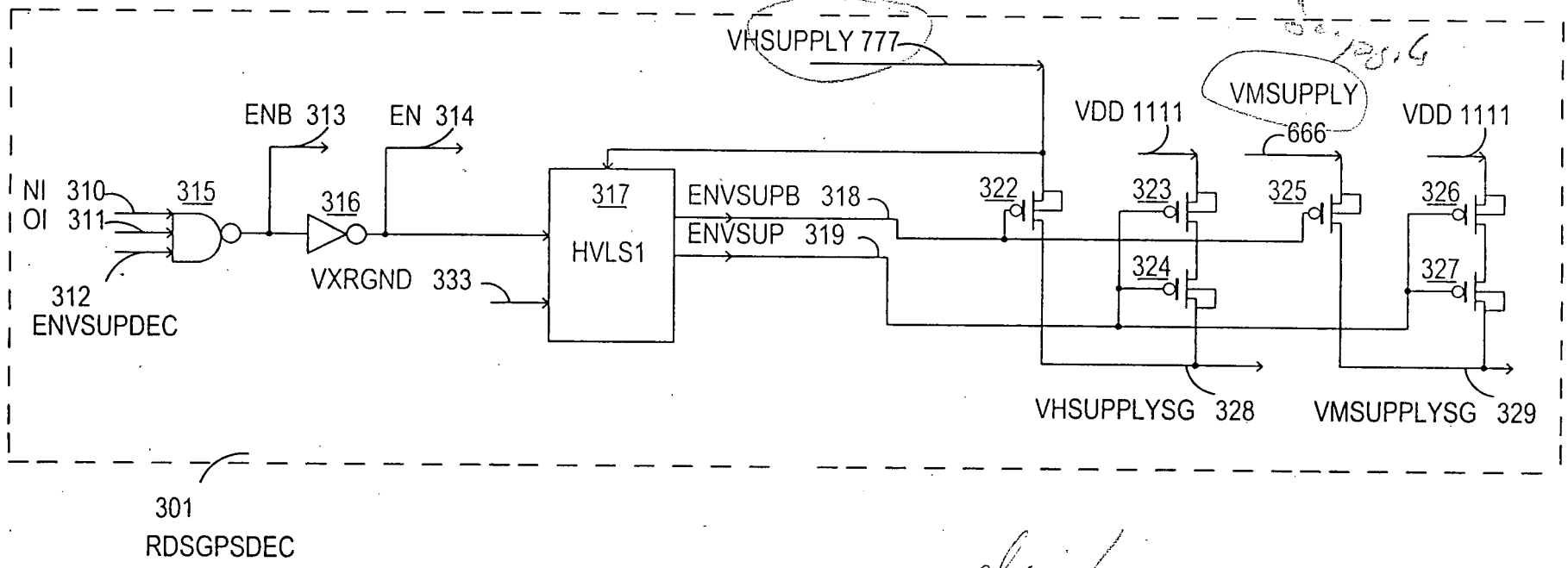


FIGURE 6 BLOCK DIAGRAM OF MULTILEVEL MEMORY DECODING



ONE SEGMENT DECODER

FIGURE 7



claim 1

SEGMENTED POWER SUPPLY DECODER FOR MULTILEVEL MEMORY DECODING

FIGURE 8

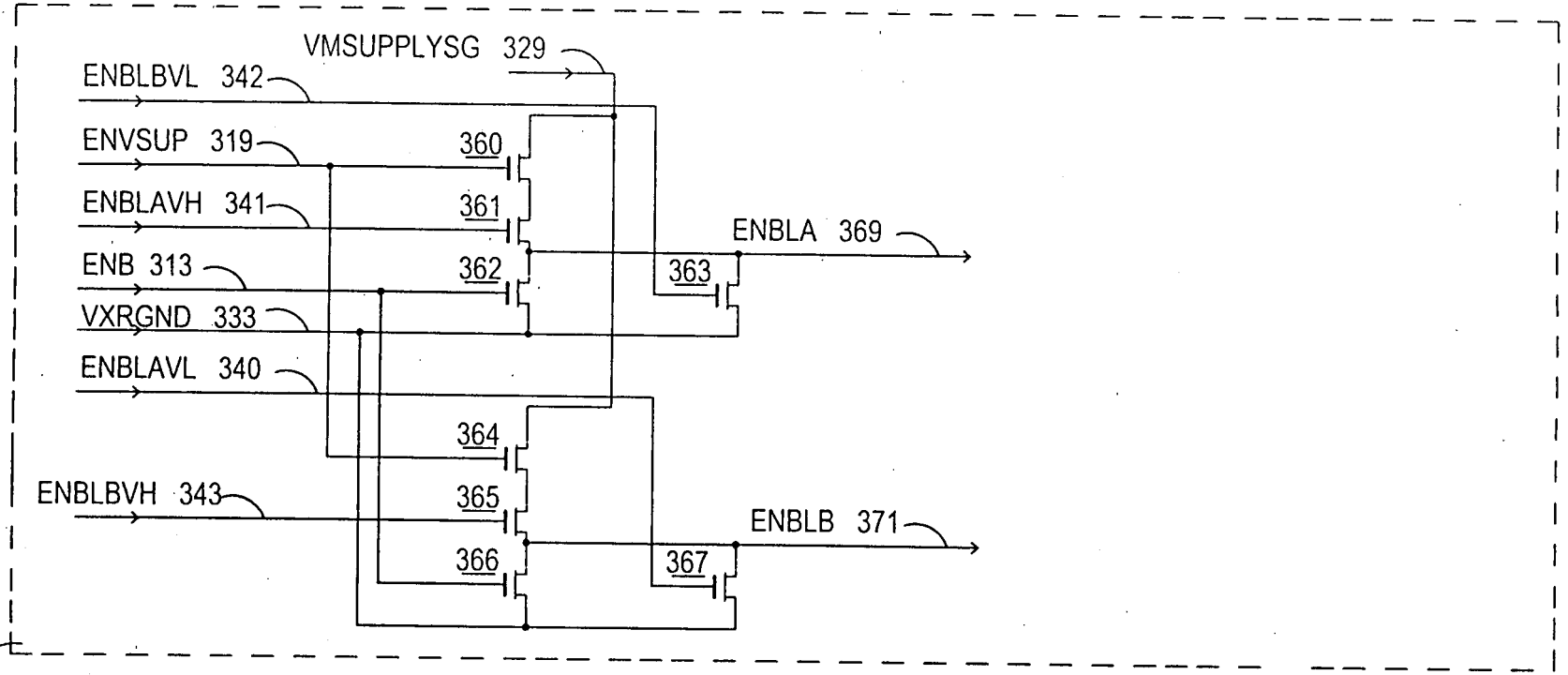


FIGURE 9A

BL SELECT DECODER FOR MULTILEVEL MEMORY DECODING

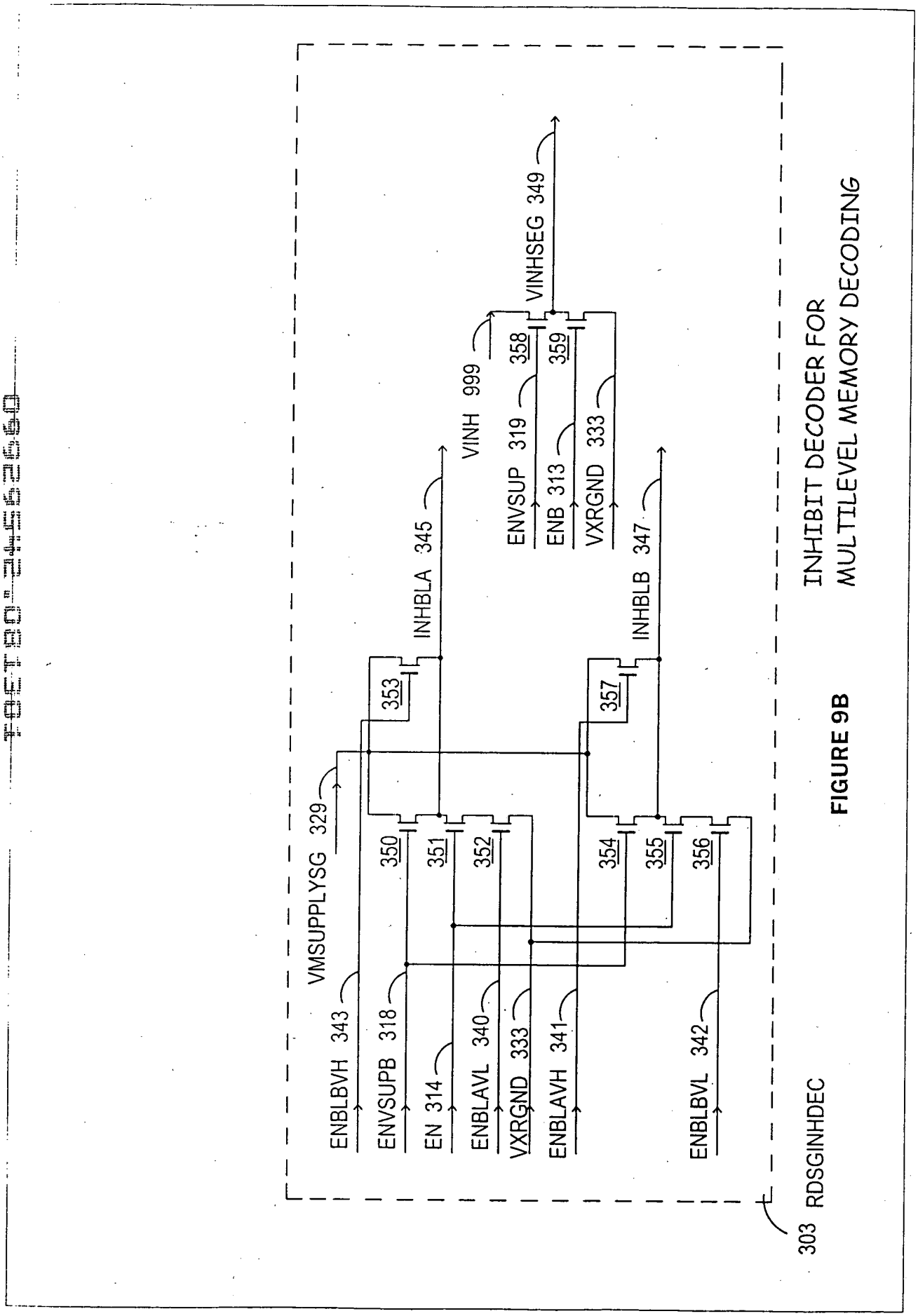


FIGURE 9B

INHIBIT DECODER FOR MULTILEVEL MEMORY DECODING

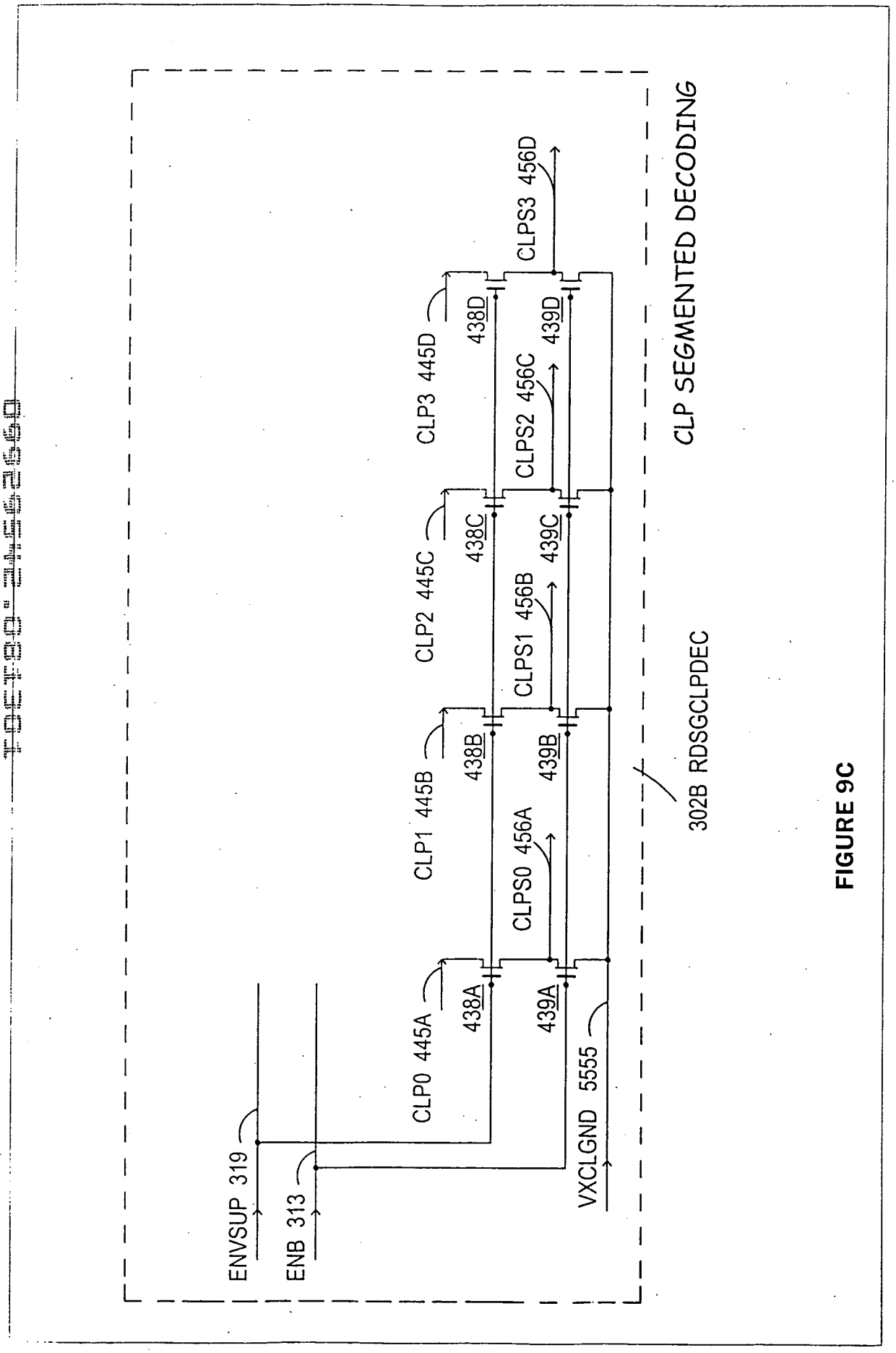

CLP SEGMENTED DECODING
302B RDSGCLPDEC
ENVSUP 319
ENB 313
CLP0 445A
CLP1 445B
CLP2 445C
CLP3 445D
438A
438B
438C
438D
439A
439B
439C
439D
CLPS0 456A
CLPS1 456B
CLPS2 456C
CLPS3 456D
VXCLGND 5555

FIGURE 9C

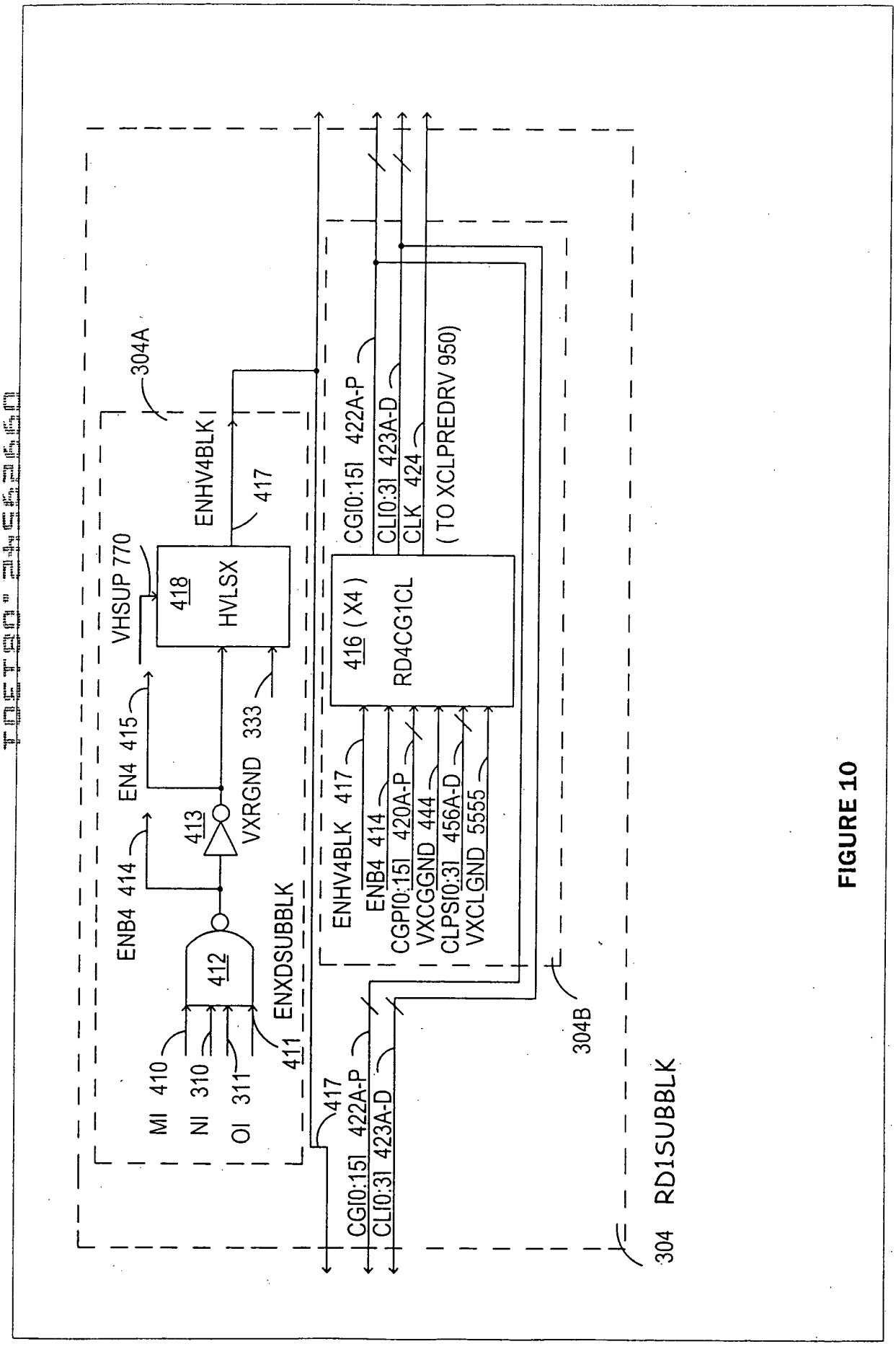

304 RD1SUBBLK
MI 410
NI 310
OI 311
411 ENXDSUBBLK
412
413
ENB4 414
EN4 415
VXRGND 333
VHSUP 770
418 HVLSX
ENHV4BLK I
417
304A
304B
ENHV4BLK 417
ENB4 414
CGP[0:15] 420A-P
VXCGGND 444
CLPS[0:31] 456A-D
VXCLGND 5555
416 (X4)
RD4CG1CL
CG[0:15] 422A-P
CL[0:31] 423A-D
CLK 424
(TO XCLPREDRV 950)
CG[0:15] 422A-P
CL[0:31] 423A-D

FIGURE 10

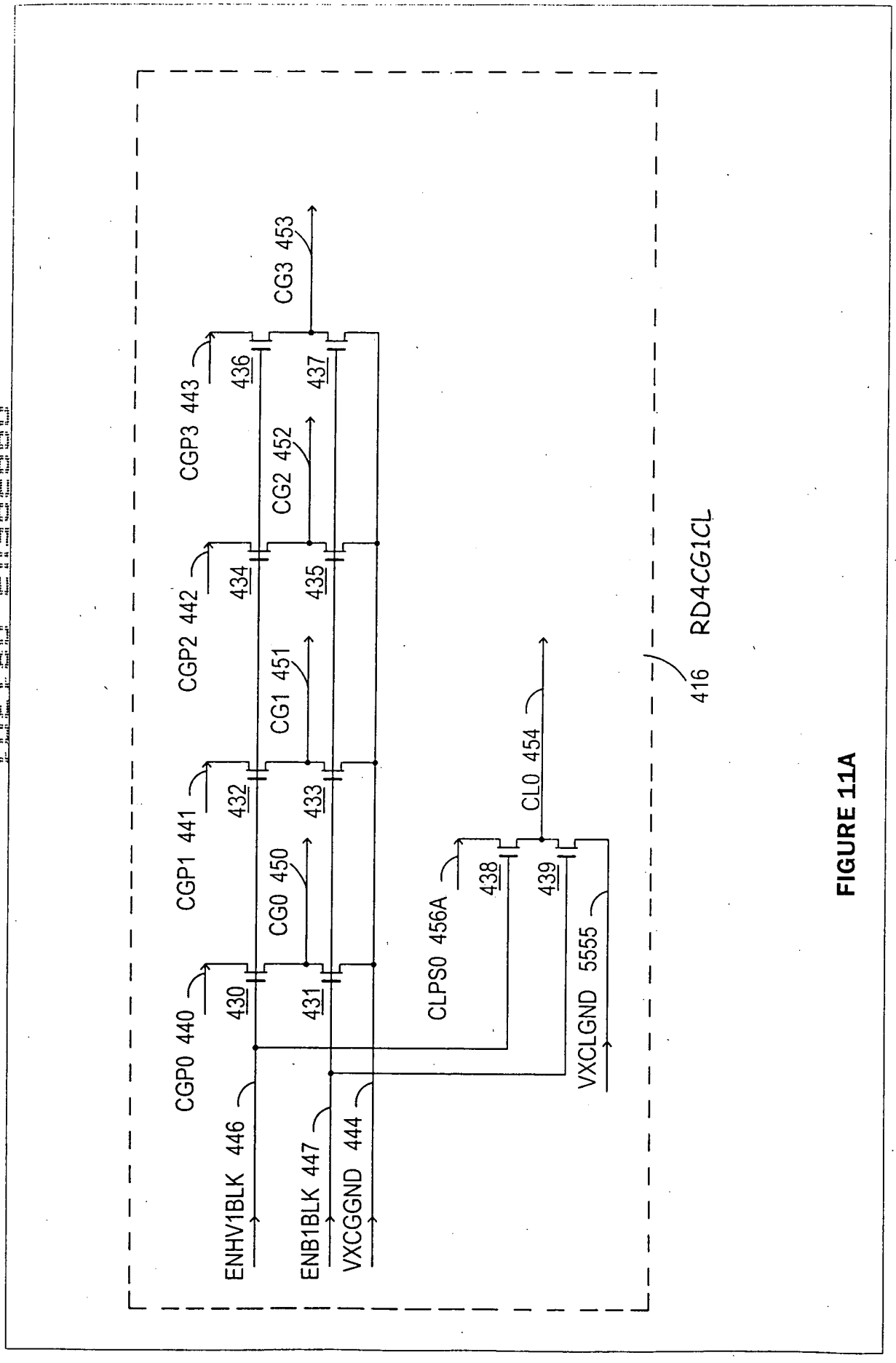

CGP0 440
CGP1 441
CGP2 442
CGP3 443
CG0 450
CG1 451
CG2 452
CG3 453
CL0 454
CLPS0 456A
ENHV1BLK 446
ENB1BLK 447
VXCGGND 444
VXCLGND 5555
430
431
432
433
434
435
436
437
438
439
416
RD4CG1CL

FIGURE 11A

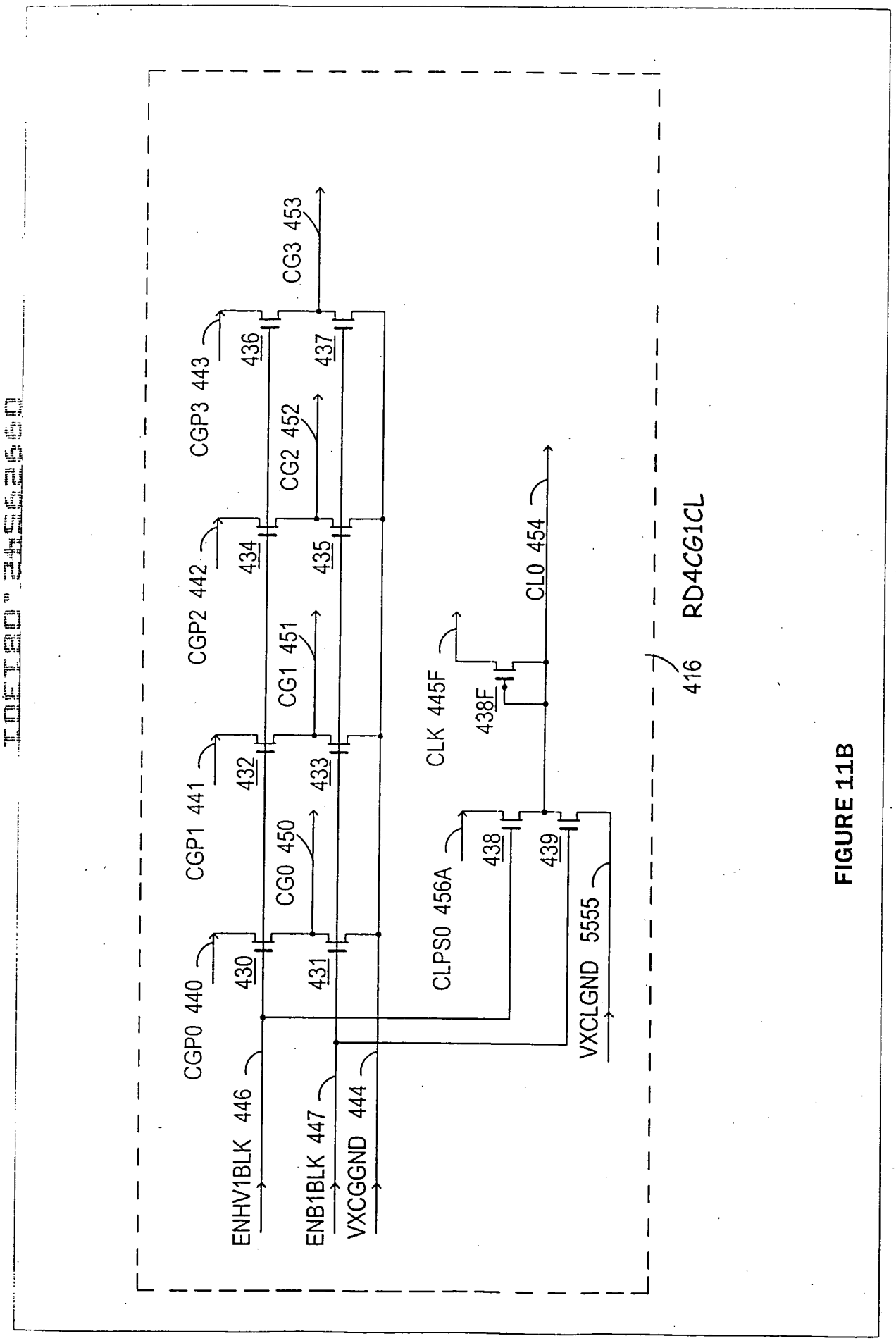

CGP0 440
CGP1 441
CGP2 442
CGP3 443
CG0 450
CG1 451
CG2 452
CG3 453
CL0 454
CLPS0 456A
CLK 445F
ENHV1BLK 446
ENB1BLK 447
VXCGGND 444
VXCLGND 5555
430
431
432
433
434
435
436
437
438
438F
439
416
RD4CG1CL

FIGURE 11B

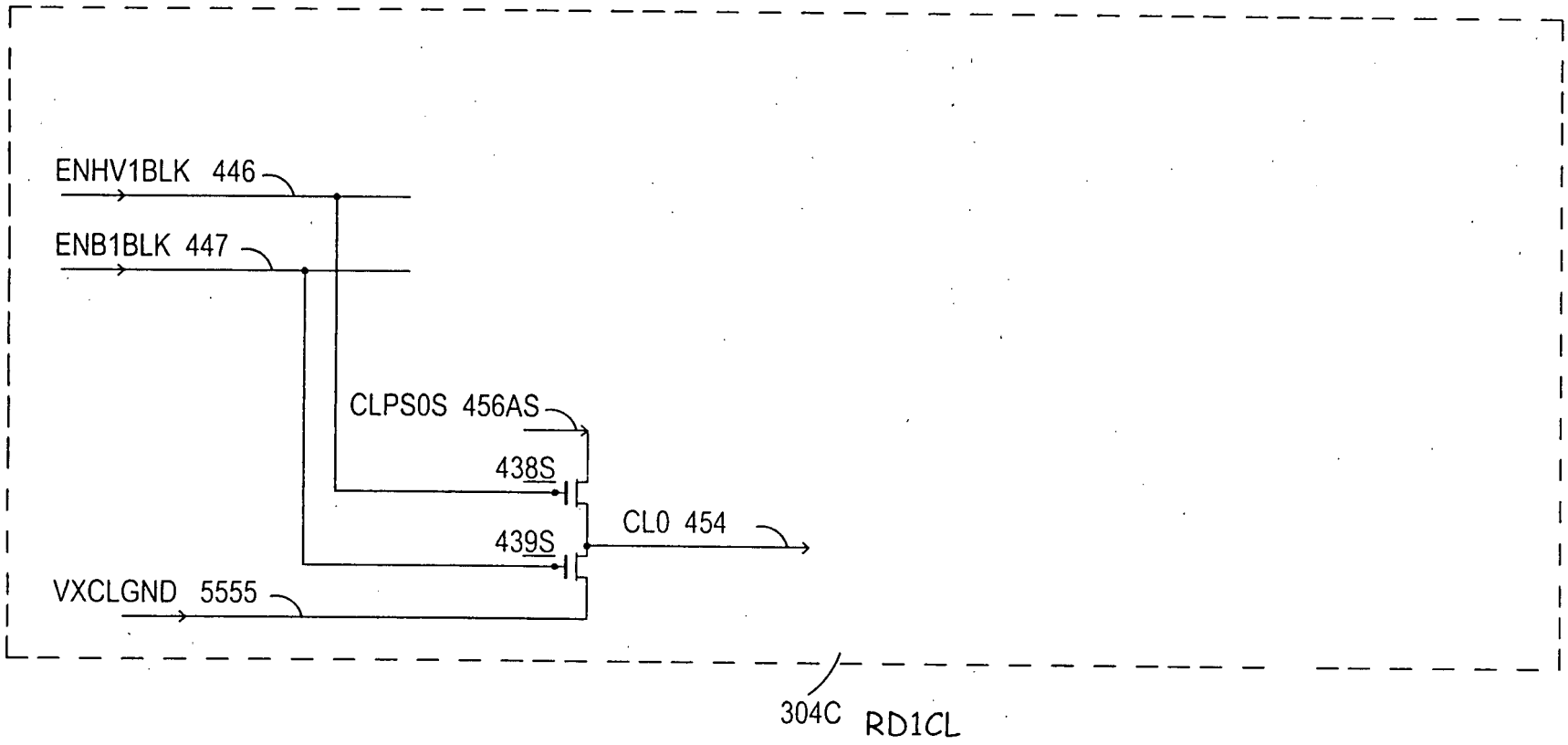
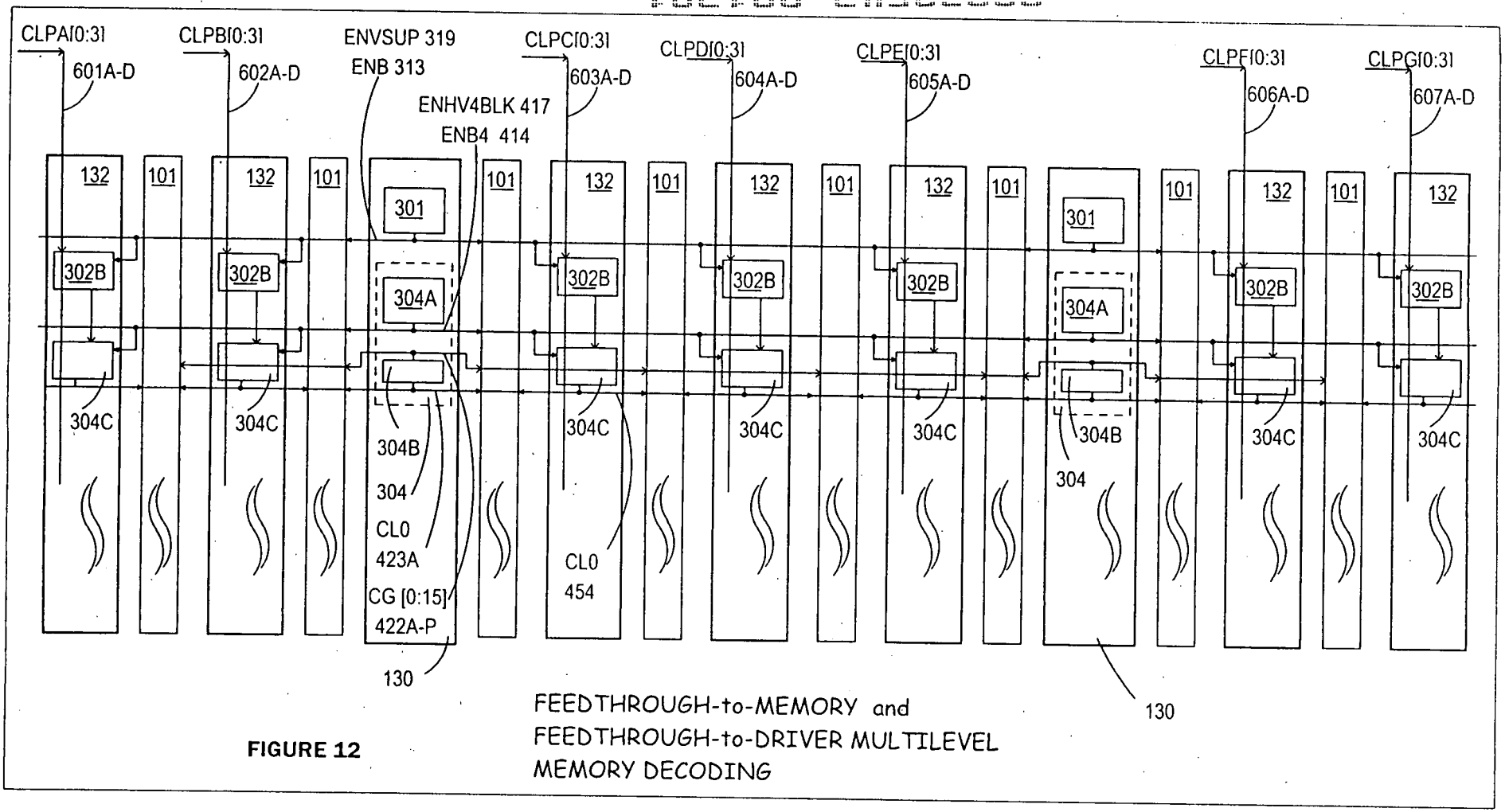
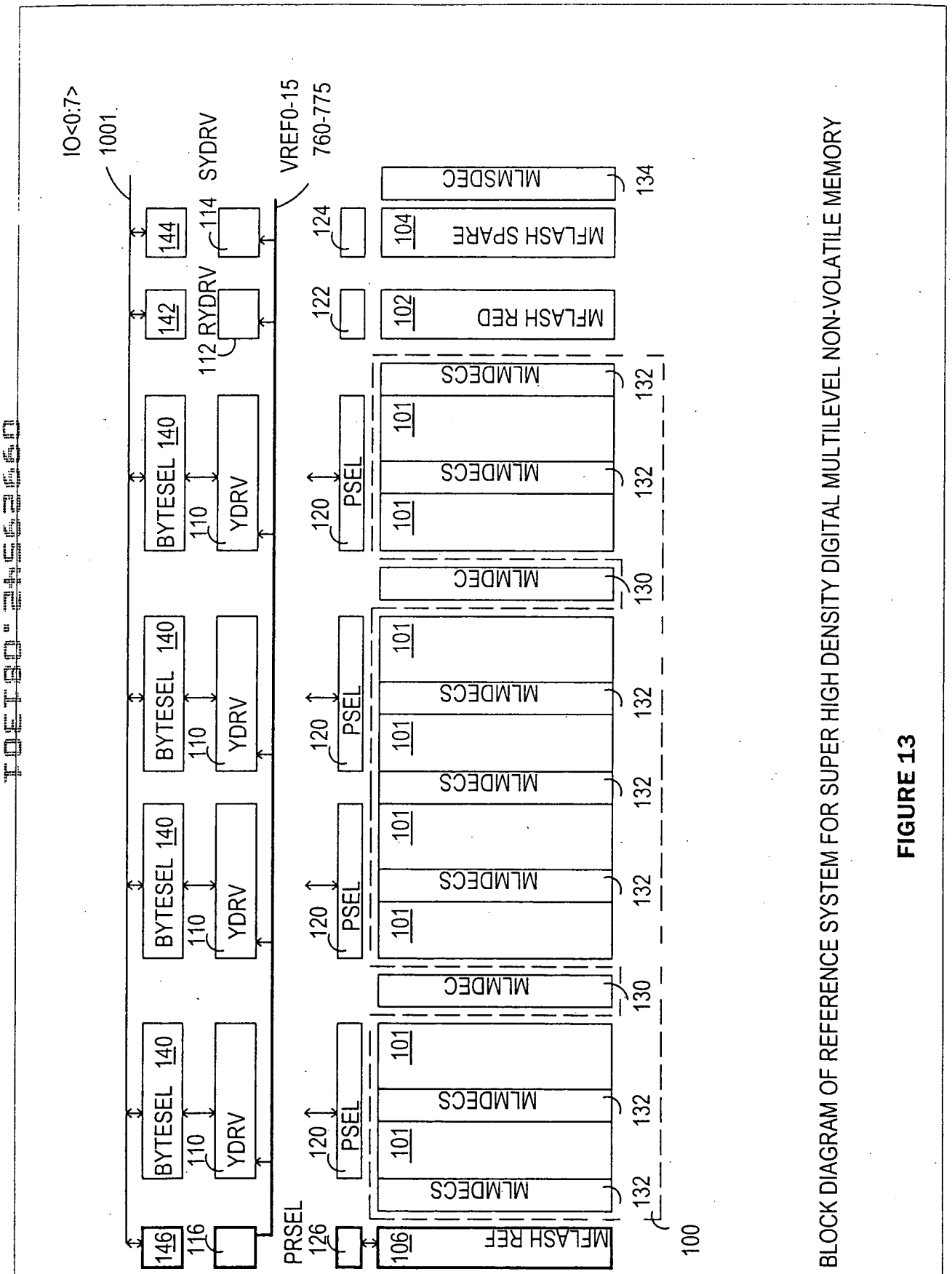

ENHV1BLK 446
ENB1BLK 447
CLPS0S 456AS
438S
439S
CL0 454
VXCLGND 5555
304C RD1CL

FIGURE 11C



FEEDTHROUGH-to-MEMORY and
FEEDTHROUGH-to-DRIVER MULTILEVEL
MEMORY DECODING

FIGURE 12



BLOCK DIAGRAM OF REFERENCE SYSTEM FOR SUPER HIGH DENSITY DIGITAL MULTILEVEL NON-VOLATILE MEMORY

FIGURE 13

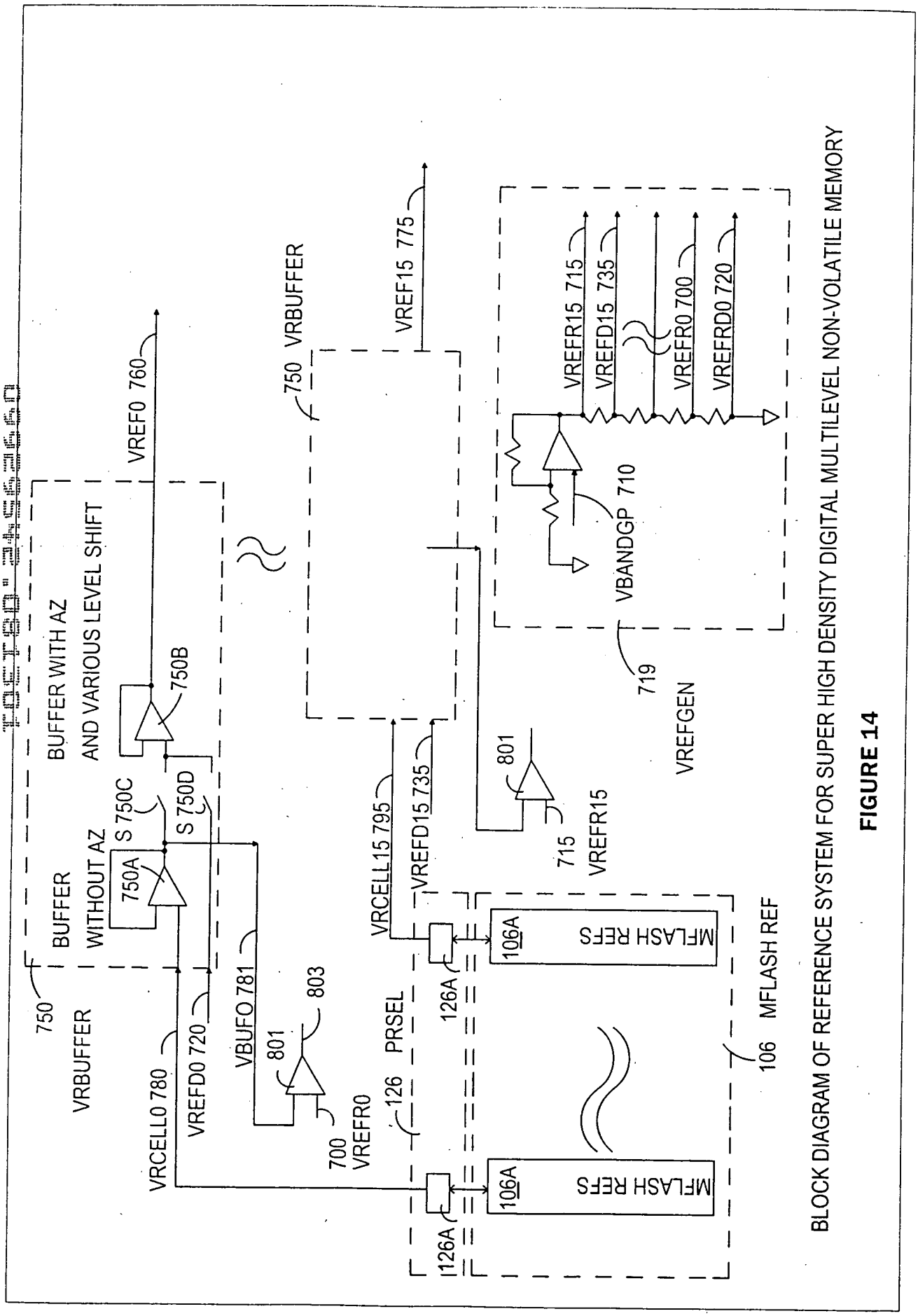
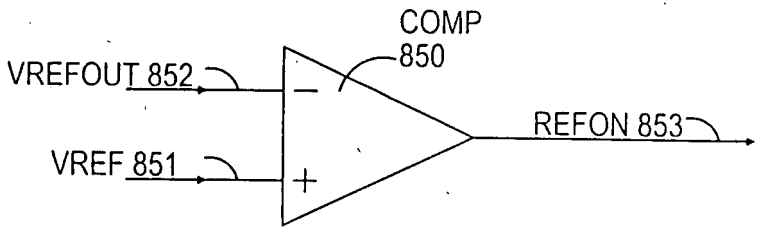


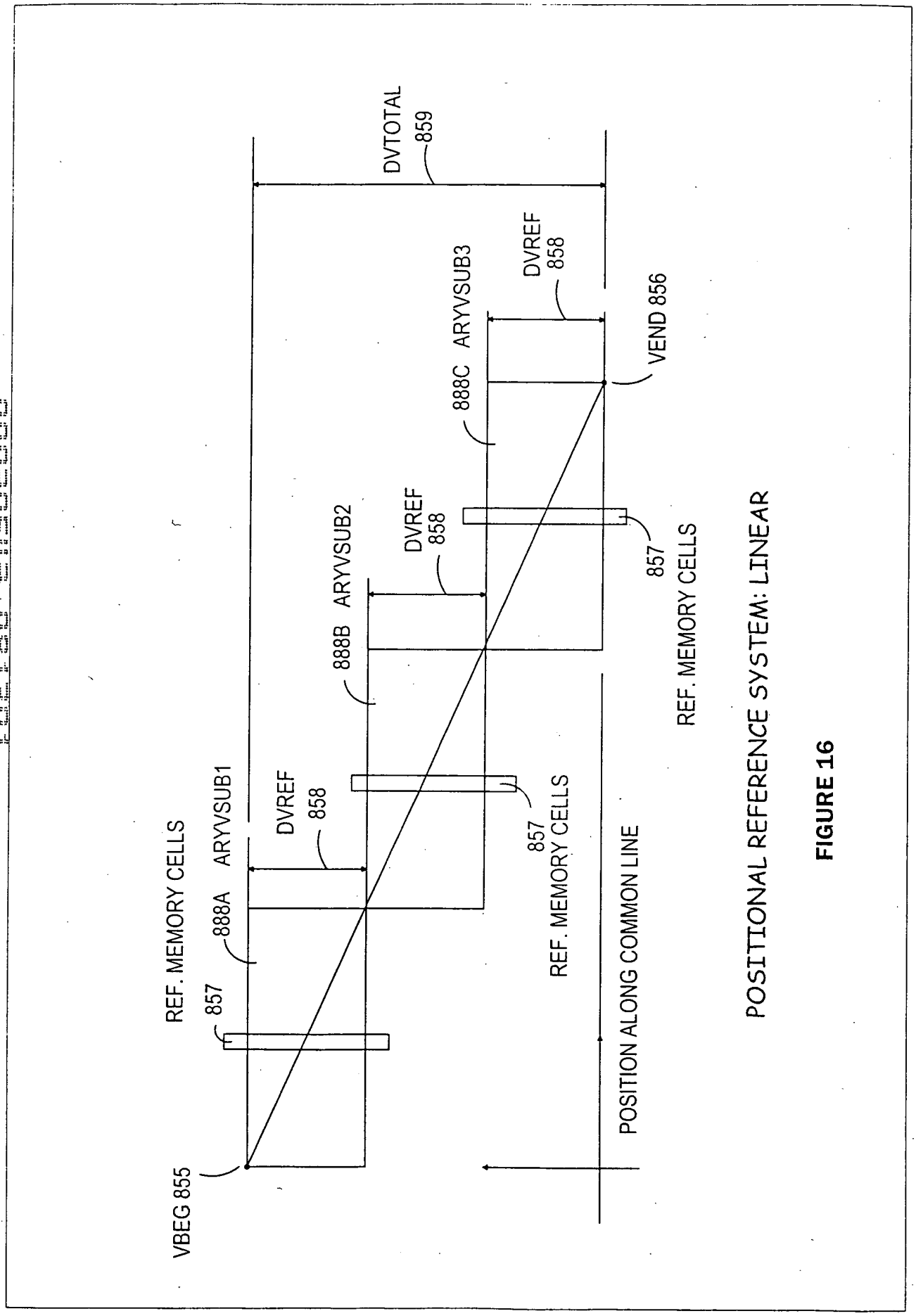
FIGURE 14

BLOCK DIAGRAM OF REFERENCE SYSTEM FOR SUPER HIGH DENSITY DIGITAL MULTILEVEL NON-VOLATILE MEMORY



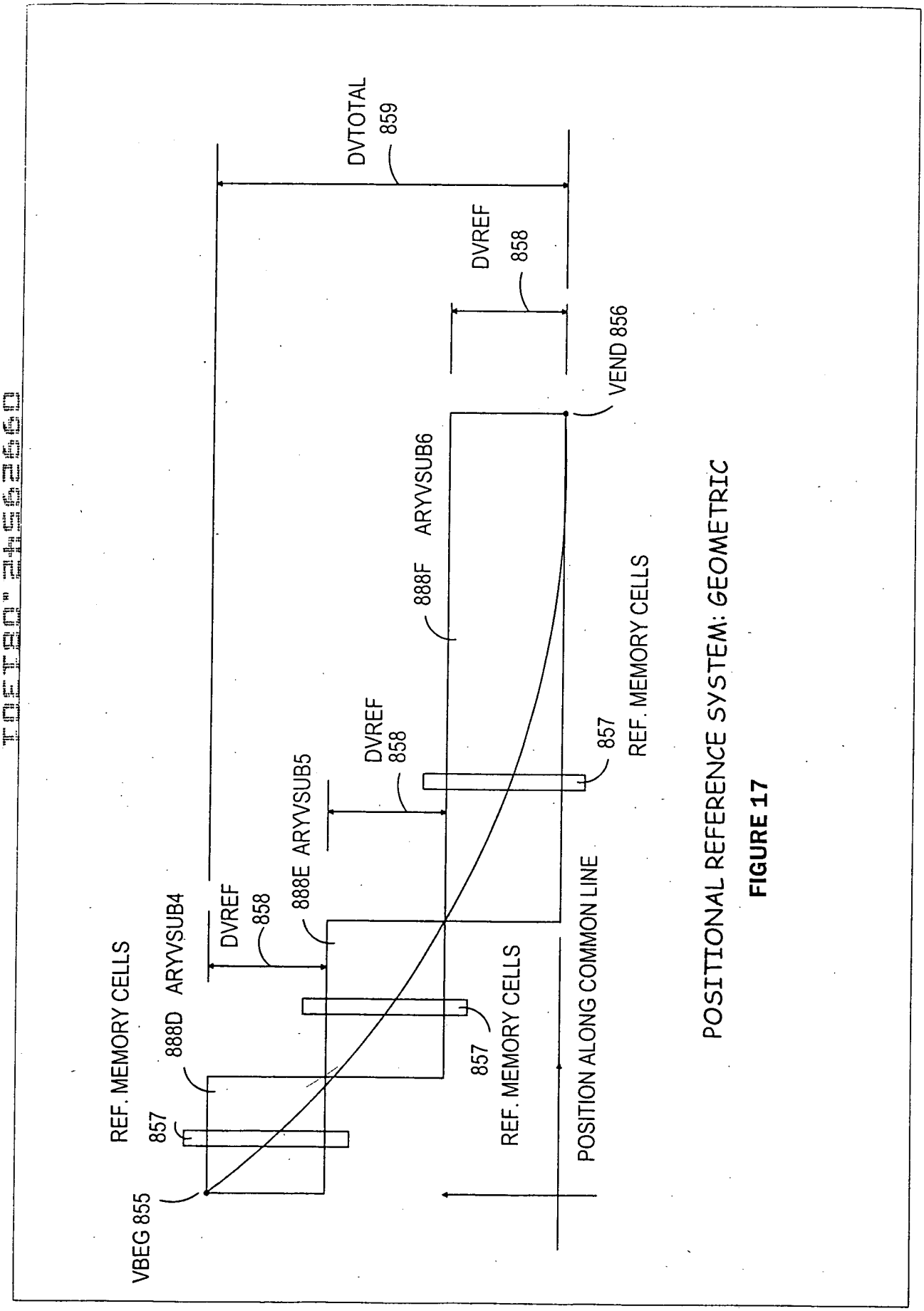
REFERENCE DETECTION

FIGURE 15



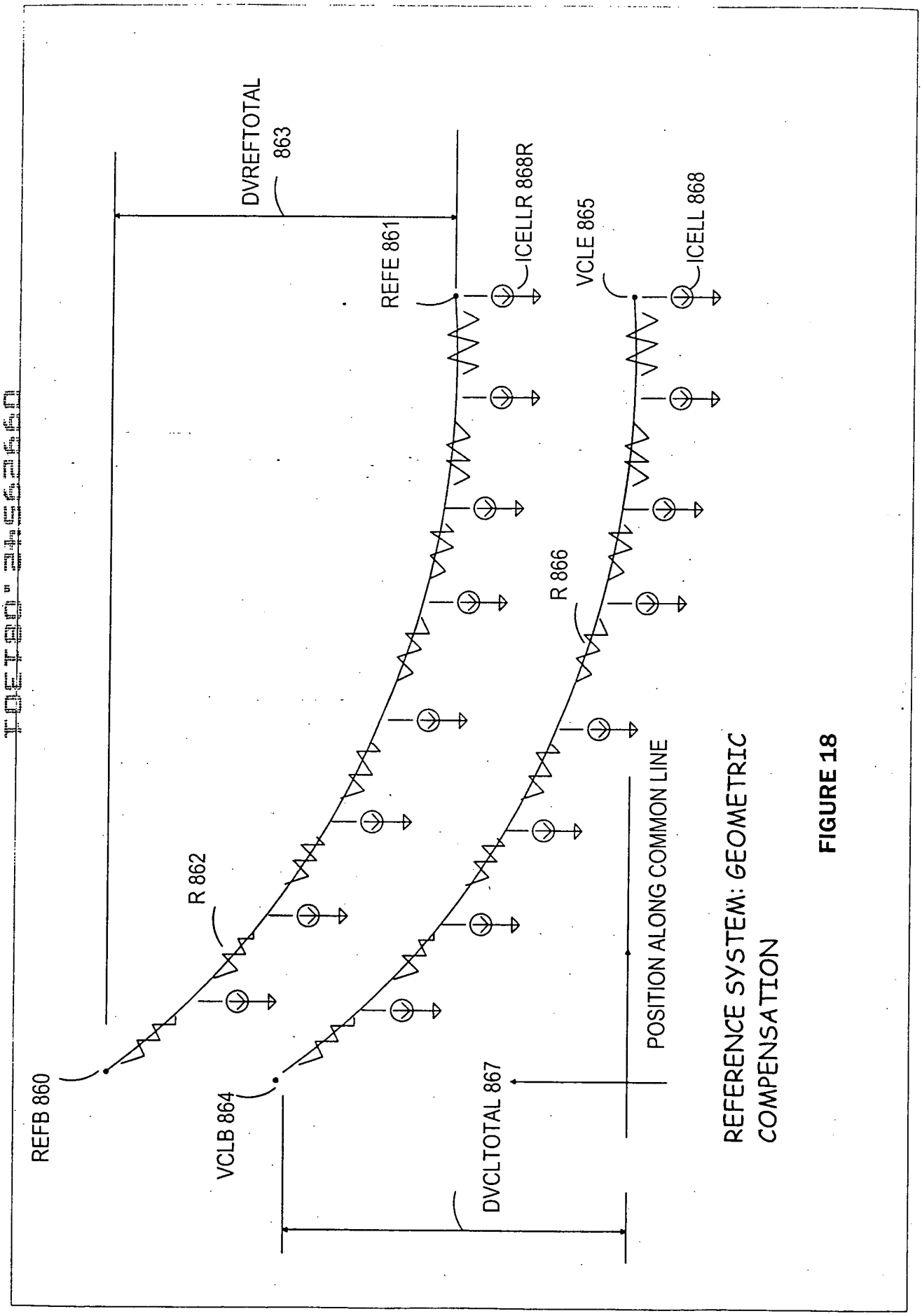
POSITIONAL REFERENCE SYSTEM: LINEAR

FIGURE 16



POSITIONAL REFERENCE SYSTEM: GEOMETRIC

FIGURE 17



REFERENCE SYSTEM: GEOMETRIC COMPENSATION

FIGURE 18

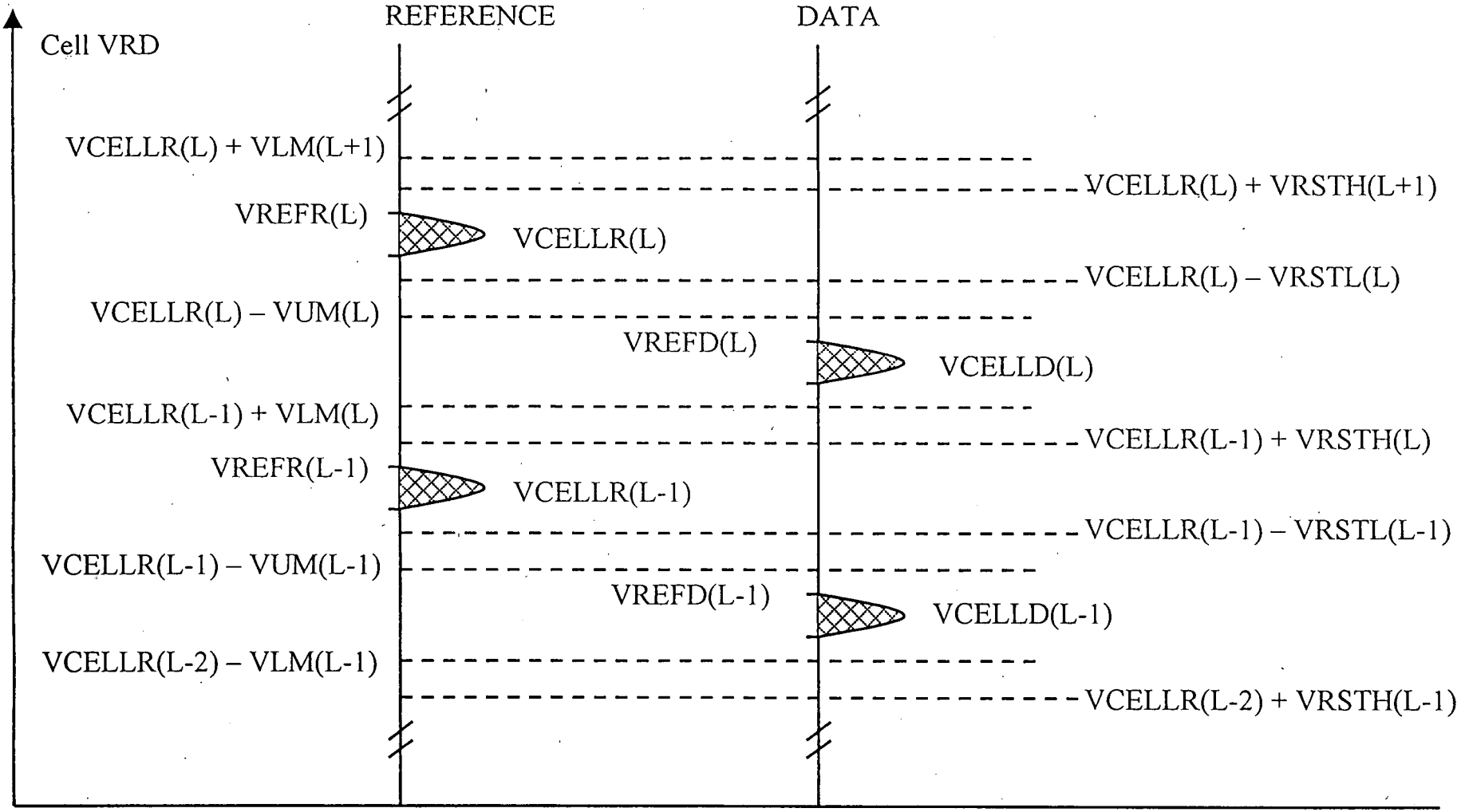


FIG._19A

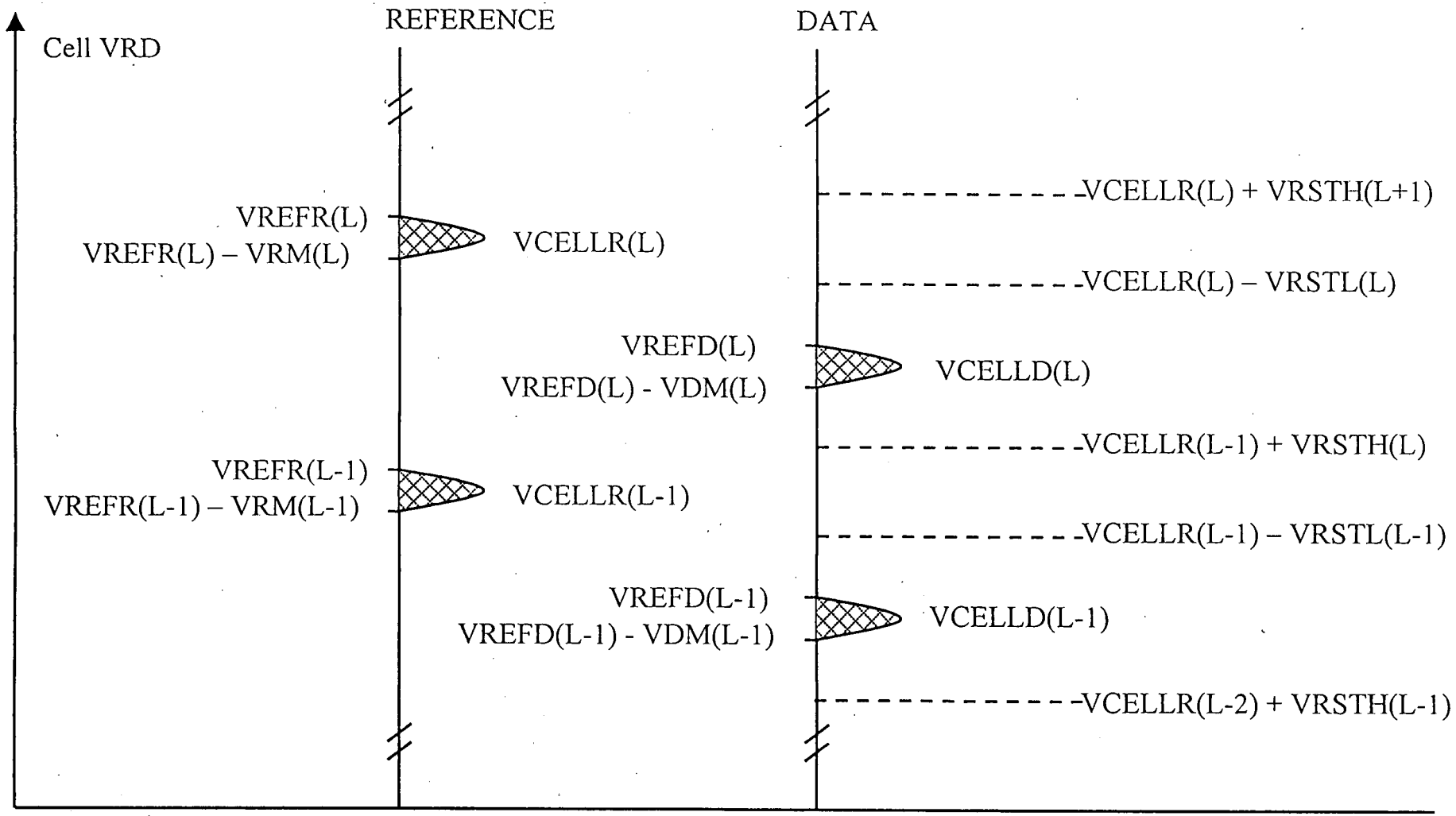

Cell VRD
REFERENCE
DATA
VREFR(L)
VREFR(L) – VRM(L)
VCELLR(L)
VCELLR(L) + VRSTH(L+1)
VCELLR(L) – VRSTL(L)
VREFD(L)
VREFD(L) - VDM(L)
VCELLD(L)
VREFR(L-1)
VREFR(L-1) – VRM(L-1)
VCELLR(L-1)
VCELLR(L-1) + VRSTH(L)
VCELLR(L-1) – VRSTL(L-1)
VREFD(L-1)
VREFD(L-1) - VDM(L-1)
VCELLD(L-1)
VCELLR(L-2) + VRSTH(L-1)

FIG._19B

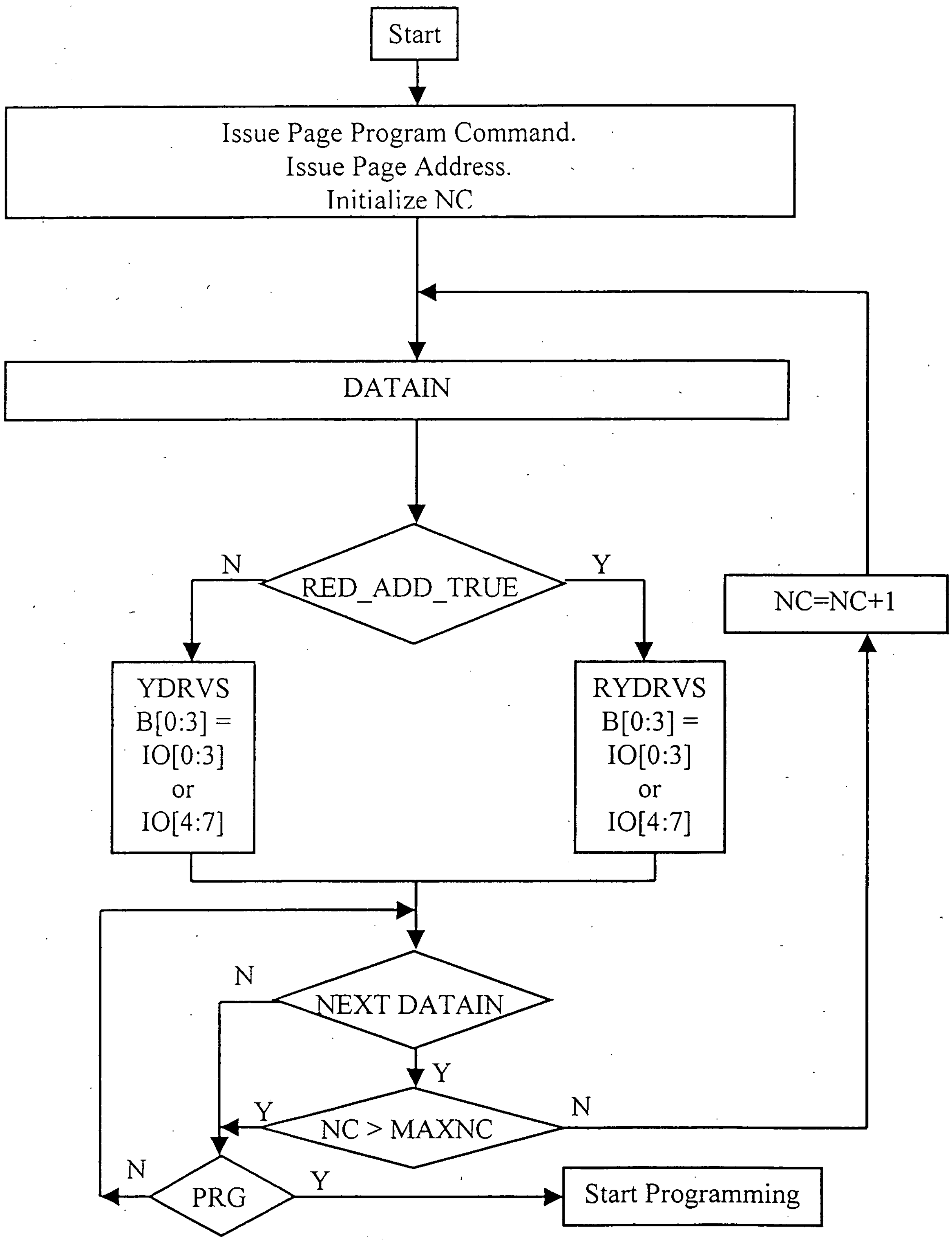


FIG._20

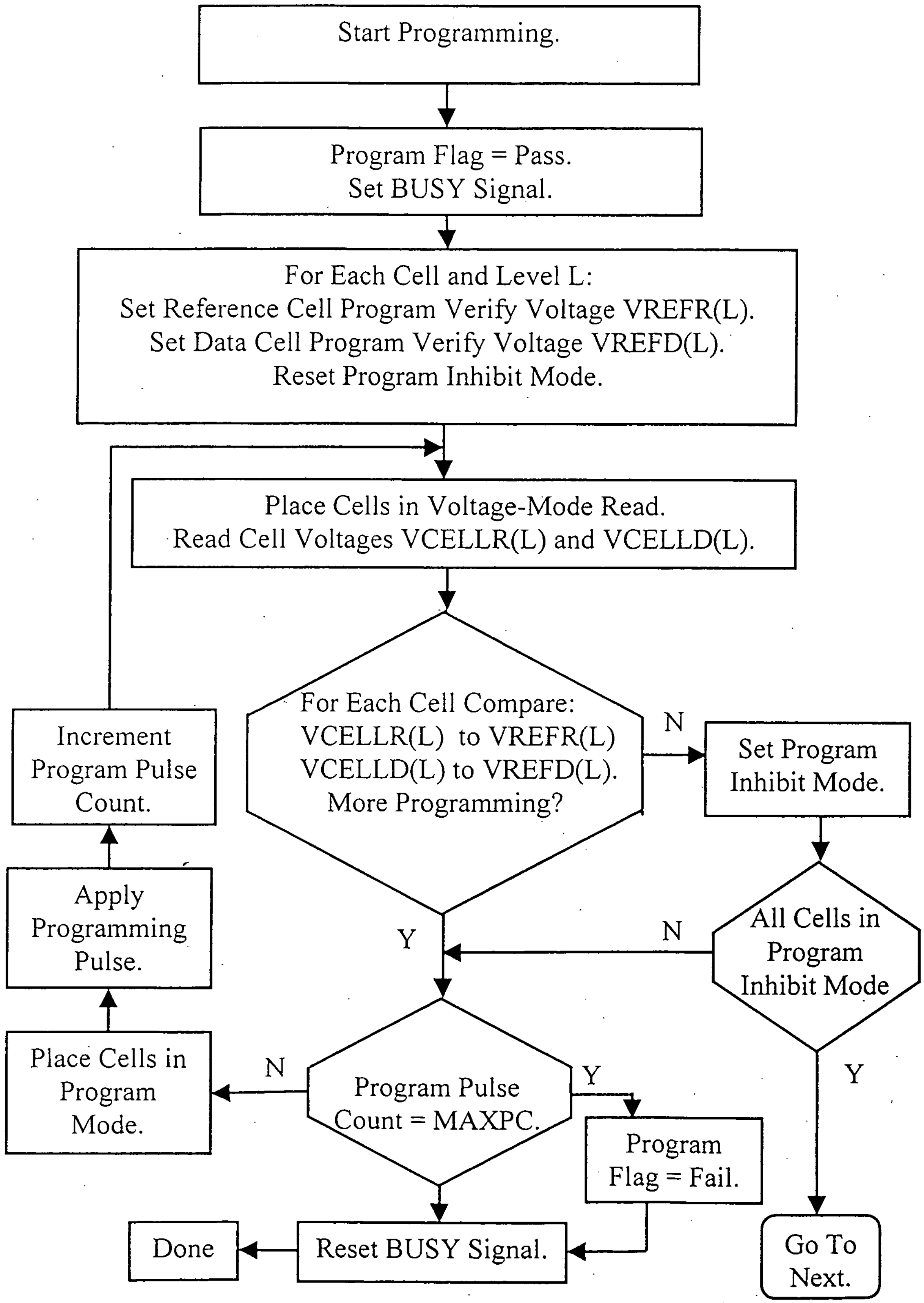


FIG._21

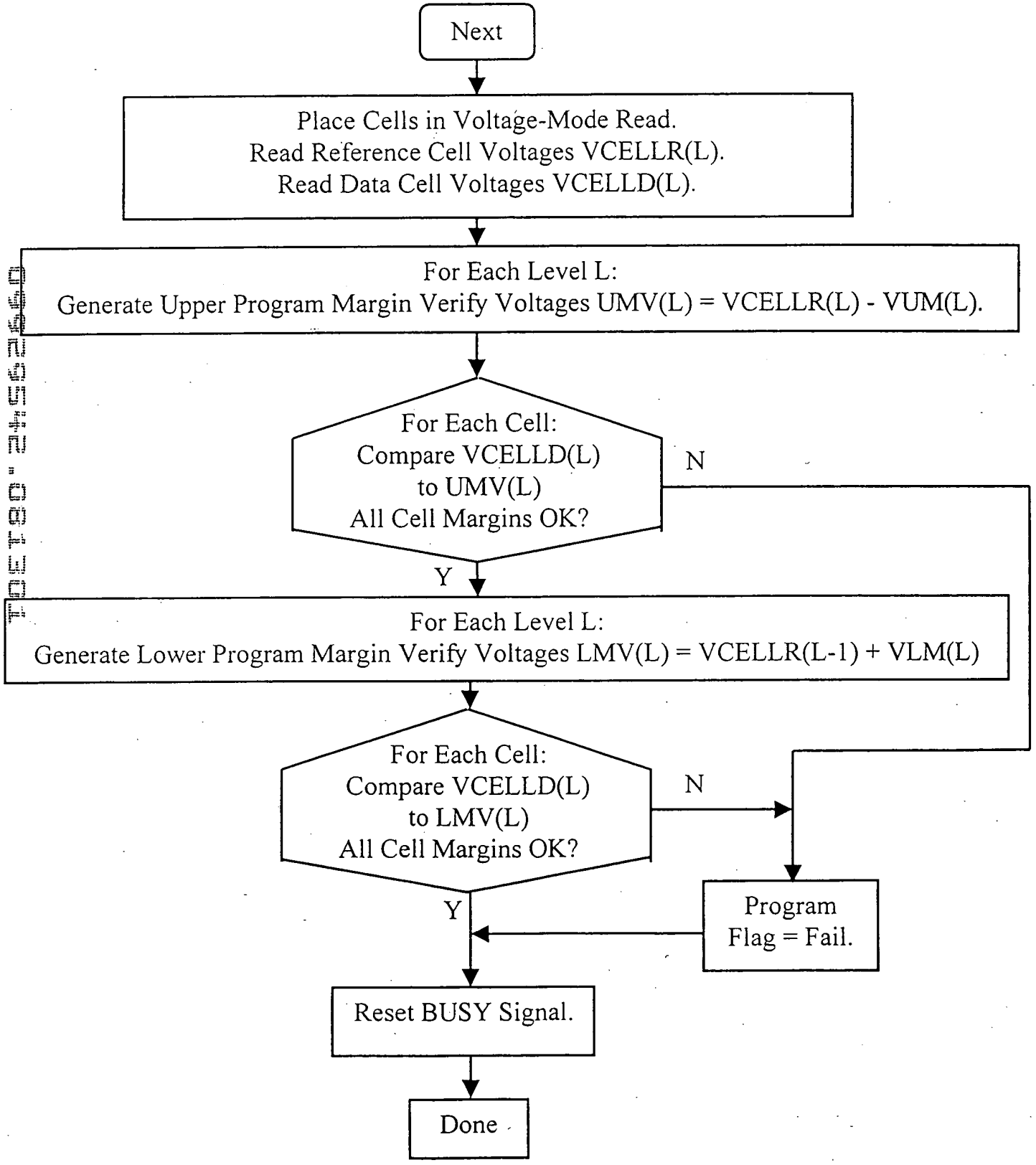

Next
Place Cells in Voltage-Mode Read.
Read Reference Cell Voltages VCELLR(L).
Read Data Cell Voltages VCELLD(L).
For Each Level L:
Generate Upper Program Margin Verify Voltages UMV(L) = VCELLR(L) - VUM(L).
For Each Cell:
Compare VCELLD(L)
to UMV(L)
All Cell Margins OK?
N
Y
For Each Level L:
Generate Lower Program Margin Verify Voltages LMV(L) = VCELLR(L-1) + VLM(L)
For Each Cell:
Compare VCELLD(L)
to LMV(L)
All Cell Margins OK?
N
Y
Program
Flag = Fail.
Reset BUSY Signal.
Done

Fig._22A

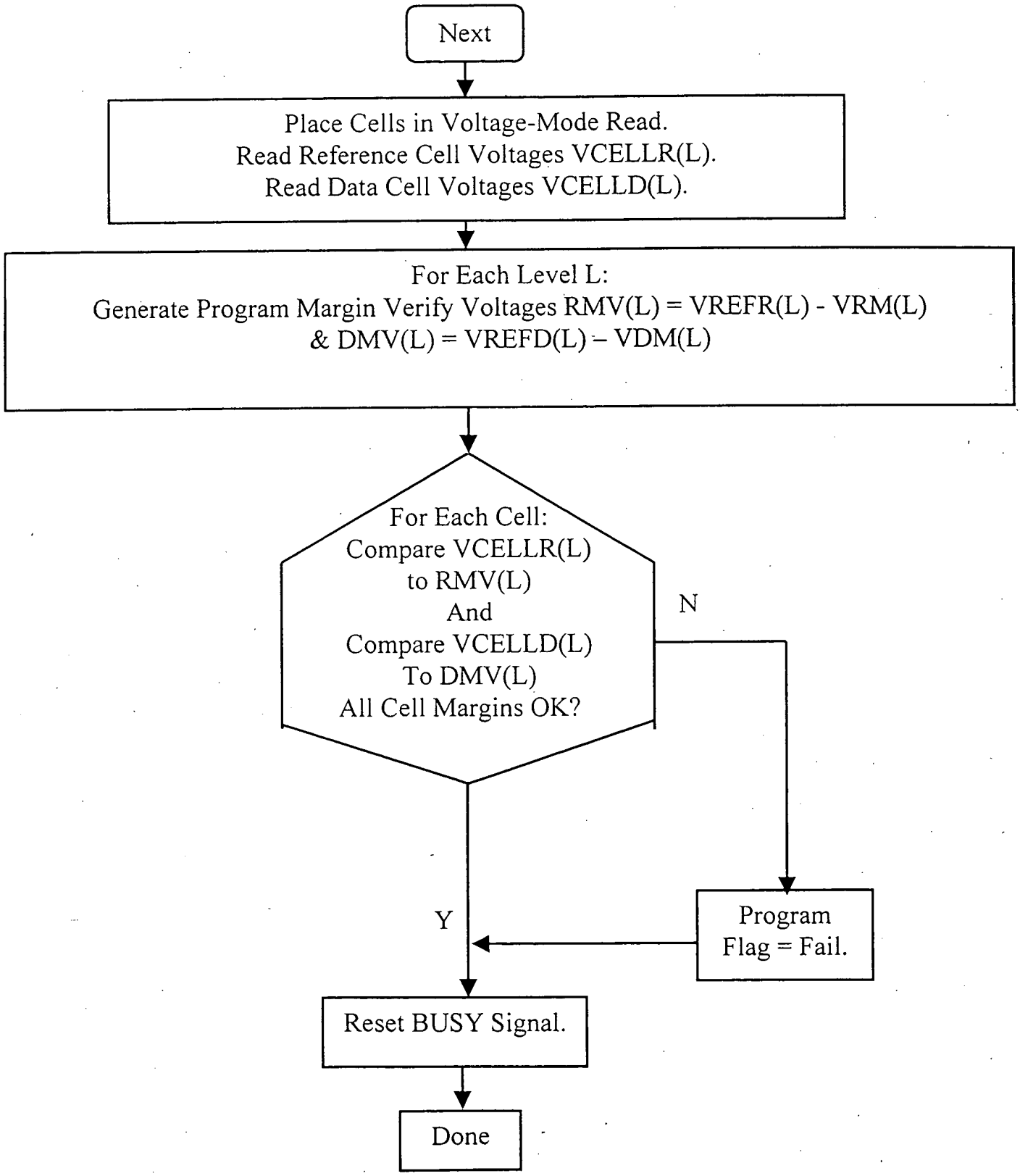

Next
Place Cells in Voltage-Mode Read.
Read Reference Cell Voltages VCELLR(L).
Read Data Cell Voltages VCELLD(L).
For Each Level L:
Generate Program Margin Verify Voltages RMV(L) = VREFR(L) - VRM(L)
& DMV(L) = VREFD(L) – VDM(L)
For Each Cell:
Compare VCELLR(L)
to RMV(L)
And
Compare VCELLD(L)
To DMV(L)
All Cell Margins OK?
N
Y
Program
Flag = Fail.
Reset BUSY Signal.
Done

Fig._22B

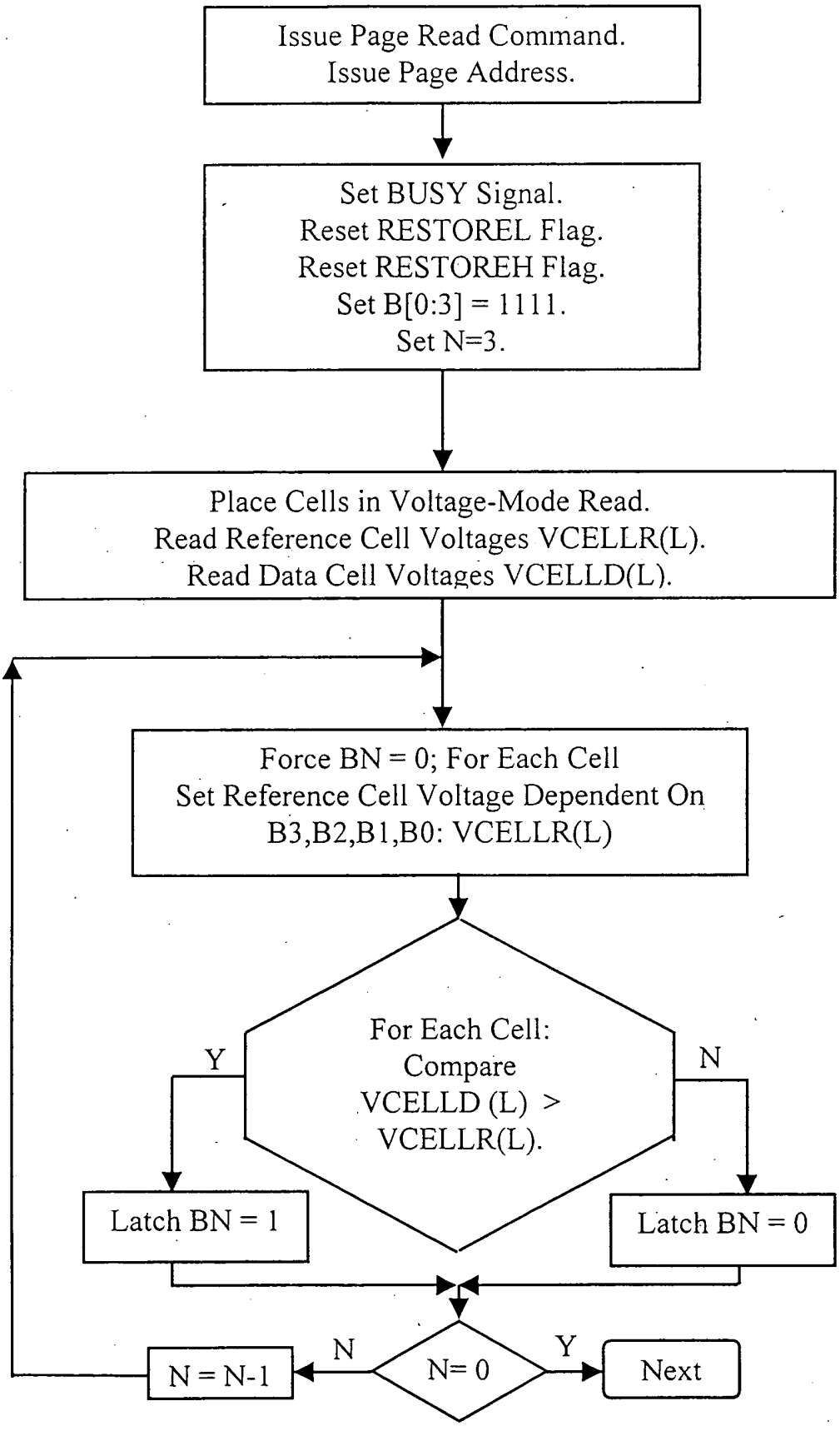

Issue Page Read Command.
Issue Page Address.
Set BUSY Signal.
Reset RESTOREL Flag.
Reset RESTOREH Flag.
Set B[0:3] = 1111.
Set N=3.
Place Cells in Voltage-Mode Read.
Read Reference Cell Voltages VCELLR(L).
Read Data Cell Voltages VCELLD(L).
Force BN = 0; For Each Cell
Set Reference Cell Voltage Dependent On
B3,B2,B1,B0: VCELLR(L)
For Each Cell:
Compare
VCELLD (L) >
VCELLR(L).
Y
N
Latch BN = 1
Latch BN = 0
N
N= 0
Y
N = N-1
Next

FIG._23

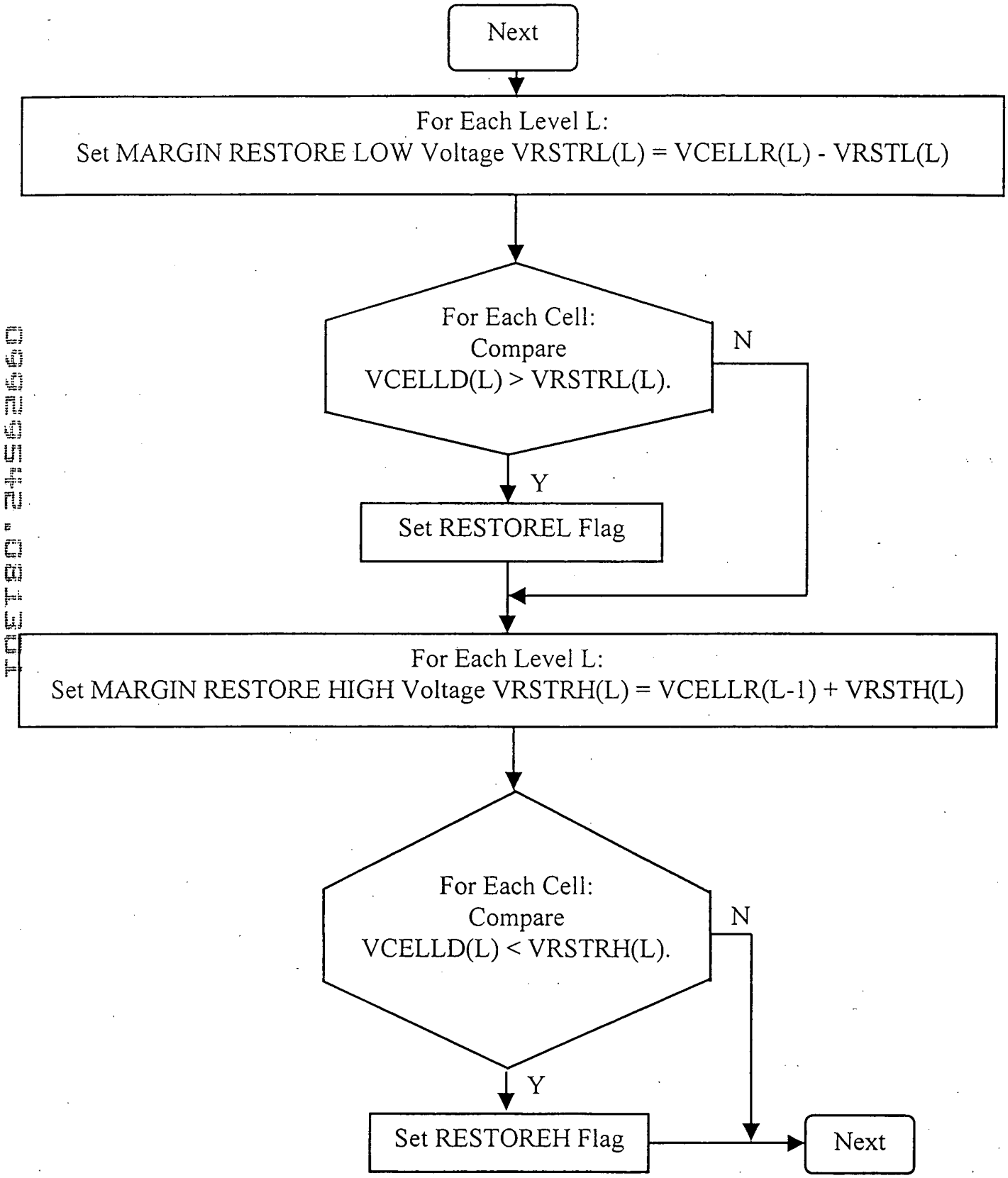

Next
For Each Level L:
Set MARGIN RESTORE LOW Voltage VRSTRL(L) = VCELLR(L) - VRSTL(L)
For Each Cell:
Compare
VCELLD(L) > VRSTRL(L).
N
Y
Set RESTOREL Flag
For Each Level L:
Set MARGIN RESTORE HIGH Voltage VRSTRH(L) = VCELLR(L-1) + VRSTH(L)
For Each Cell:
Compare
VCELLD(L) < VRSTRH(L).
N
Y
Set RESTOREH Flag
Next

FIG._24

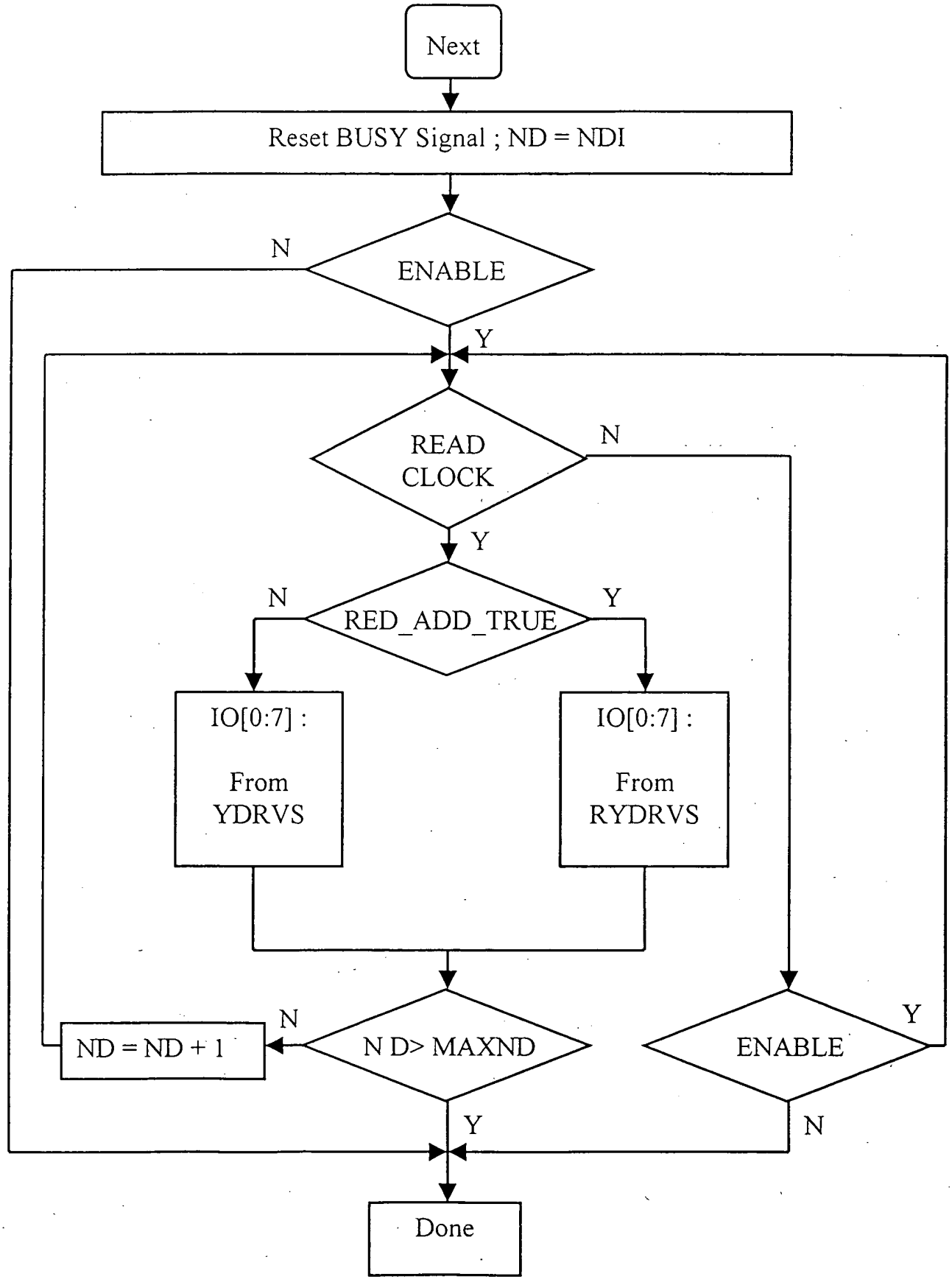

Next
Reset BUSY Signal ; ND = NDI
ENABLE
N
Y
READ CLOCK
N
Y
RED_ADD_TRUE
N
Y
IO[0:7] : From YDRVS
IO[0:7] : From RYDRVS
N D> MAXND
N
ND = ND + 1
ENABLE
Y
N
Y
Done

FIG._25

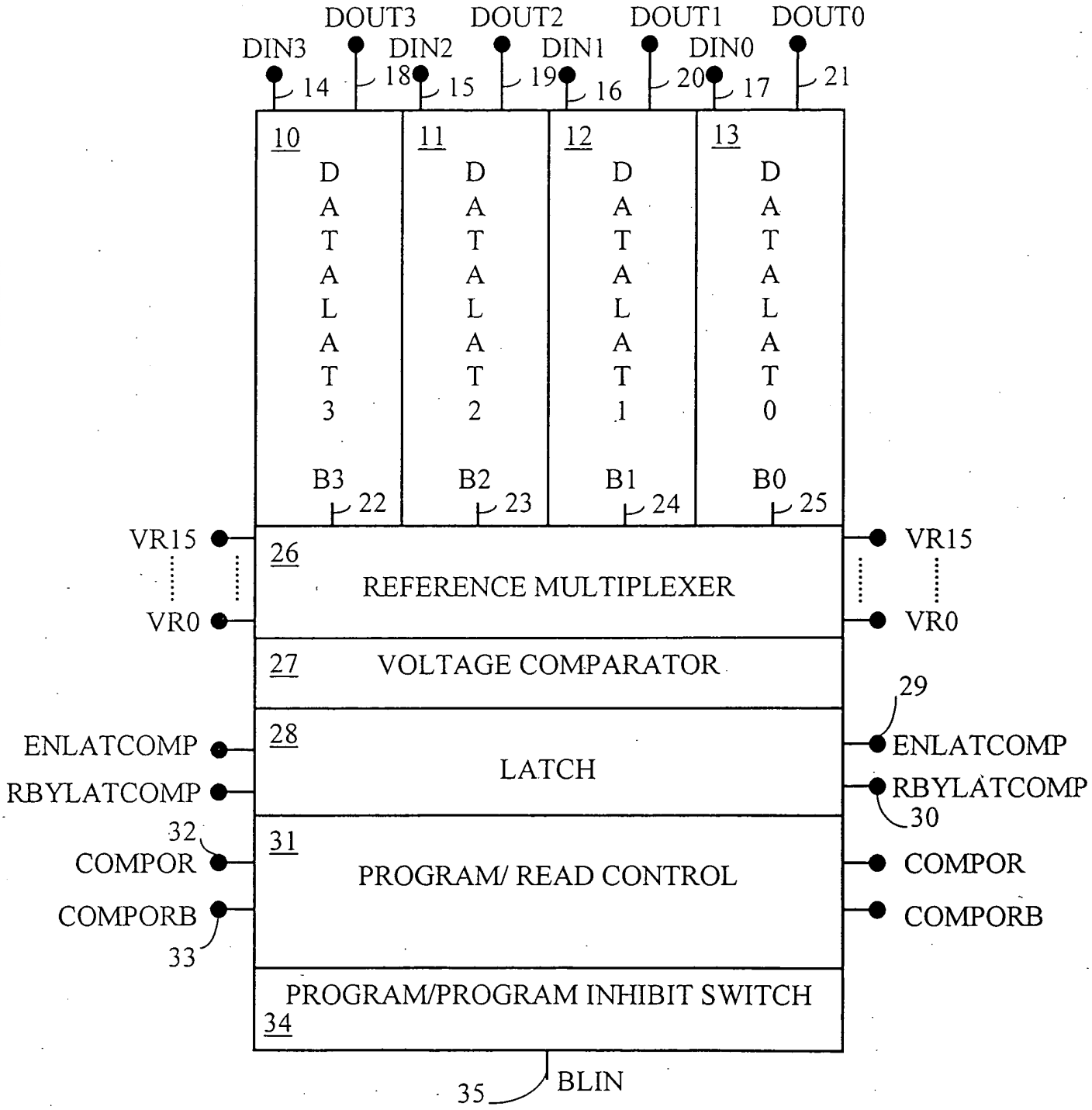

DOUT3
DOUT2
DOUT1
DOUT0
DIN3
DIN2
DIN1
DIN0
14
18
15
19
16
20
17
21
10
11
12
13
DATALAT3
DATALAT2
DATALAT1
DATALAT0
B3
B2
B1
B0
22
23
24
25
VR15
VR0
26
REFERENCE MULTIPLEXER
27
VOLTAGE COMPARATOR
29
28
ENLATCOMP
RBYLATCOMP
LATCH
30
32
31
COMPOR
COMPORB
PROGRAM/ READ CONTROL
33
PROGRAM/PROGRAM INHIBIT SWITCH
34
35
BLIN

Fig._26

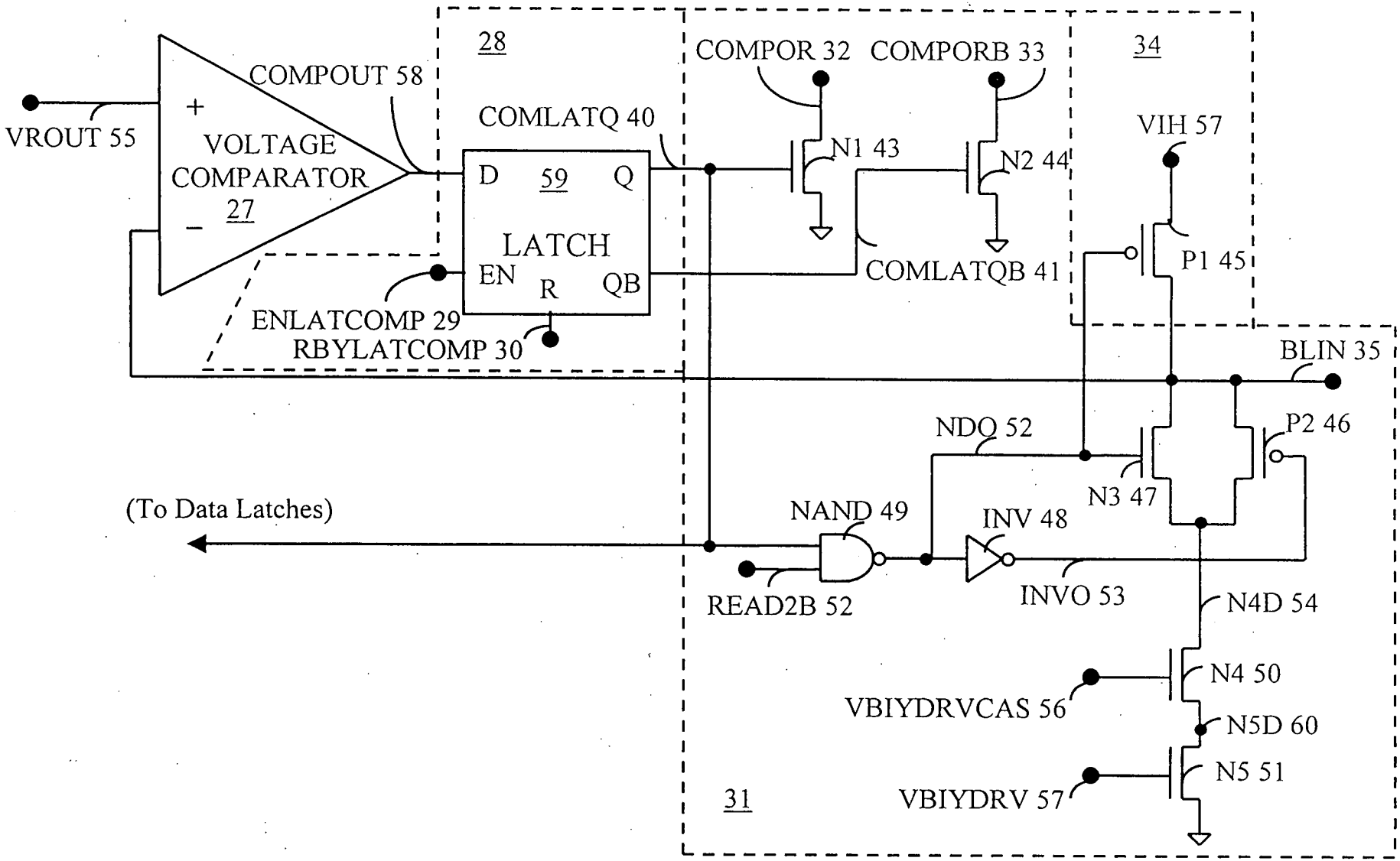

28
COMPOR 32
COMPORB 33
34
COMPOUT 58
COMLATQ 40
VIH 57
VROUT 55
+
VOLTAGE
COMPARATOR
27
−
D
59
Q
LATCH
EN
R
QB
N1 43
N2 44
COMLATQB 41
P1 45
ENLATCOMP 29
RBYLATCOMP 30
BLIN 35
NDQ 52
P2 46
N3 47
(To Data Latches)
NAND 49
INV 48
READ2B 52
INVO 53
N4D 54
N4 50
VBIYDRVCAS 56
N5D 60
N5 51
31
VBIYDRV 57

Fig._27